# Influence of Quantum Dot Characteristics on the Performance of Hybrid SET-FET Circuits

E. Amat, F. Klüpfel, J. Bausells, *Senior Member, IEEE*, and F. Perez-Murano

***Abstract*— Quantum dots (QDs) can be used as conductive islands to build-up single-electron transistors (SETs). The characteristics of the QDs define the functional performance of the SETs. In consequence, analyzing the influence of the variations of QD dimensions on the performance of hybrid SET-FET circuits is of high relevance. We employ a self-developed SET compact model which is calibrated to 3-D quantum-mechanics-based simulations in order to obtain realistic model parameters. A method to improve the circuit behavior, i.e., to increase the output current, is proposed. It is concluded that the variation of the QD size presents the largest influence on the overall circuit behavior.**

***Index Terms*— Nanowires, quantum dot (QD), single-electron transistor (SET), variability.**

## I. Introduction

QUANTUM dots (QDs) are gaining relevance for the development of new device approaches for future nanoelectronics. QDs can be made of a small conducting or semiconducting particle, usually below 10 nm size. A QD located between two conducting surfaces forms a single-electron transistor (SET) provided that a third electrode allows to properly tuning the energy levels of the system. The advantages of this device concept are already known for many years [1]. For instance, SETs can achieve ultralow power consumption for technology nodes beyond 10 nm [2], [3]. A SET exhibits Coulomb blockade (CB) due to progressive charging of the QD with electrons which block subsequent electrons by electrostatic repulsion from entering the QD. For SETs with metallic QDs, the orthodox theory of single-electron tunneling is frequently used to describe the CB oscillations [1]. The tunneling junctions are then modeled by the capacitance in parallel with the resistance.

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E. Amat, J. Bausells, and F. Perez-Murano are with the Institute of Microelectronics of Barcelona (IMB-CNM, CSIC), 08193 Bellaterra, Spain (e-mail: esteve.amat@imb-cnm.csic.es).

F. Klüpfel is with the Department of Modeling and Artificial Intelligence, Fraunhofer Institute for Integrated Systems and Device Technology (IISB), 91058 Erlangen, Germany.

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While significant benefits are provided by SETs, e.g., low power consumption, several limitations threaten their practical application, e.g., background charge noise, low drive current, device stability, and the requirement for ultralow temperature operation if the QD in not small enough. Background charge noise promotes the implementation of silicon-based SETs because the use of nonmetallic QDs minimizes the random charge near the SET island that affects the device behavior [4], [5]. Furthermore, the cointegration with a conventional field-effect transistor (FET) can overcome its low output drive current because the FET device amplifies the current provided by the SET. SET-FET hybrid circuits combine the benefits of SETs (ultralow power consumption and low dimensions) and FETs (high speed and voltage gain), allowing the designing of circuits with enhanced functionality [5]. The monolithic integration of SET and FET requires that the fabrication of both devices is based on compatible methods [6]. Finally, by reducing the QD dimensions below 10 nm, operation at room temperature is feasible [5].

According to the requirement of the semiconductor industry of increasing integration density, and so reducing device dimensions, conventional metal oxide FETs (MOSFETs) are discarded for SET-FET circuits as their reliability is highly affected due to unacceptable leakage currents and large device performance variability [7]. Then, vertical nanowire FETs arise as the most promising candidate [8], due to their low area footprint, high device performance, and low variability level.

Several works have addressed the realization of room temperature SETs [6], [9]. In particular, vertical nanowire SETs have been studied in [10], which allows for a relevant benefit on area footprint reduction, although its operation has not been demonstrated at room temperature. A disruptive proposal to implement a SET is by using a nanopillar structure formed by a thin oxide layer embedded in the pillar, where a silicon nanocrystal is generated by ion beam mixing and subsequent annealing [11]. Experimentally, fabrication of self-aligned silicon QDs in a $SiO_2$ layer via ion beam mixing has been demonstrated for QD diameters in the 3-nm range [11]. In our previous study [12], we showed that large driving currents and low variability is obtained when the SET-FET circuit is implemented by using vertical nanowire as an FET device.

The main objective of the present contribution is to investigate the influence of the QD position and dimensions on the final hybrid circuit behavior, in order to analyze the impact of the QD variability on the performance of the SET-FET circuit.

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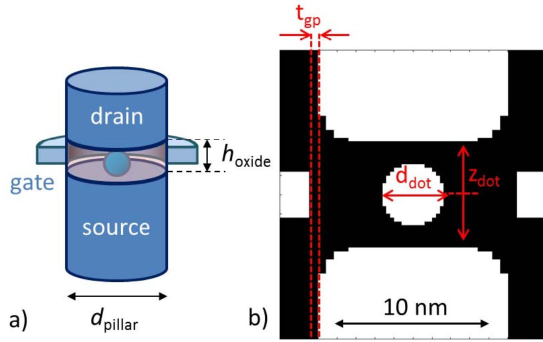


Fig. 1. (a) Schema of a SET based on a silicon nanopillar with embedded oxide layer. (b) Cross-sectional scheme through the 10-nm pillar SET simulated in this article, where the SET dimensional parameters are depicted.

The remainder of this article is organized as follows. Section II presents the device models to simulate the hybrid circuit and the simulation environment. Section III studies the impact of the QD position in a single SET and in a SET-FET. Section IV explores the variability impact on the hybrid circuit. Section V summarizes the conclusions of the analysis.

## II. SET-FET Simulation Framework

This section describes the hybrid SET-FET circuit simulations and the conditions of the analysis that has been performed.

### A. Definition of the SET and FET Device Characteristics

We present the behavioral simulation of a vertical SET. In particular [see Fig. 1(a)], our SET is based on a vertical silicon pillar topology, where the QD is generated within an embedded $SiO_2$ layer (6 nm thick). Its performance has been evaluated previously by 3-D quantum–mechanics-based simulations [13]. For circuit analysis, a compact model is necessary that allows the efficient evaluation of the SET characteristics. Existing SET compact models require electrical parameters like tunneling resistance and capacitance values. Thus, they do not allow studying the influence of geometrical quantities or material properties. In order to allow the analysis of circuit properties as a function of geometry variations, we have developed a compact model, based on the work of Inokawa and Takahashi [3]. In the following, we describe the adjustments and additions to the compact model necessary to describe 3-D simulations of silicon-pillar-based SETs. The 3-D simulations are based on the commercial Schroedinger/Poisson solver nextnano++ with additional post-processing steps to calculate tunneling currents based on the transfer Hamiltonian approach introduced by Bardeen [14]. Coulomb interaction of carriers on the QD is implemented in a mean-field approach. Exchange interactions are respected by nextnano++ via the local spin density approximation presented in [15]. Further details about the 3-D simulation approach can be found in [13]. It should be noted that the effective-mass approximation used by nextnano++ has reduced accuracy for QD sizes below 5 nm, and e.g., overestimates the effective bandgap of the QD [16]. However, general trends of the QD properties with respect to QD size are still preserved and allow the investigation of SET variability even if the absolute values of currents and voltages might deviate somewhat from the expected experimental results.

We vary the geometrical properties as well as external parameters like voltage and temperature. Fig. 1(b) schematizes the relevant QD dimensions: 1) vertical position ($z_{\mathrm{dot}}$); 2) size ($d_{\mathrm{dot}}$); and 3) gate-to-pillar distance ($t_{\mathrm{gp}}$). The nominal values of these parameters are: $z_{\mathrm{dot}} = 0.0$ nm, $d_{\mathrm{dot}} = 3.2$ nm, and $t_{\mathrm{gp}} = 0.7$ nm. The QD size complies with the target of room-temperature operation [1] and the experimental results for QD fabrication presented in [11].

In the original model of Inokawa and Takahashi [3], the current as a function of the gate voltage consists of a series of overlapping bell-shaped peaks. Derived in [3] is the characteristic of a single current peak $I_n$ which describes the tunneling current when the electron number on the QD fluctuates between $n$ and $n+1$. The electron number on the QD depends on the external voltages and is given in the SPICE model by the expression

$$n = \mathrm{int}\left(\frac{C_{\mathrm{g}} V_{\mathrm{gs}}}{e} + \frac{C_{\mathrm{b}} V_{\mathrm{bs}}}{e} - (C_{\mathrm{g}} + C_{\mathrm{b}} + C_{\mathrm{s}} - C_{\mathrm{d}}) * \frac{V_{\mathrm{ds}}}{2e}\right). \tag{1}$$

Here, $C_{\mathrm{g}}$, $C_{\mathrm{b}}$, $C_{\mathrm{s}}$, and $C_{\mathrm{d}}$ denote the capacitances between QD and the contacts gate, bulk–source, and drain, respectively. Please note that no bulk contact exists in the pillar-SET geometry. Thus, bulk-QD capacitance $C_{\mathrm{b}}$ and bias $V_{\mathrm{bs}}$ are assumed to be zero in the following. The int($x$) function returns the nearest integer lower or equal to $x$. For the compact model, the current peak derived by Inokawa and Takahashi [3] is duplicated along $V_{\mathrm{gs}}$ by introducing a normalized gate voltage $\tilde{V}_{\mathrm{gs}}$ proportional to $C_{\mathrm{g}} V_{\mathrm{gs}}/e - n$. This results in a sawtooth-like $\tilde{V}_{\mathrm{gs}}$ characteristic that facilitates the repetition of $I_n$ along $V_{\mathrm{gs}}$, resulting in a periodical characteristic for the whole gate voltage range. The derivation of $n$ and $\tilde{V}_{\mathrm{gs}}$ is presented in more detail in [17].

The most prominent effect covered by the model presented in this article in contrast to previous SET compact models is the off-regime, which originates from the bandgap of the silicon QD (compare Fig. 2). The off-regime is introduced by restricting the electron number $n$ given by (1) to either zero or positive values. A further adjustment is the shortening of the first oscillation period after the threshold, which is due to a difference in the shape of the electrostatic potential for the uncharged QD in comparison to the charged one. This effect can be included in the compact model by using a 60% larger gate capacitance value for the first current peak $I_0$ after the threshold in comparison to the following oscillation periods. The peak shape in the device characteristics is strongly influenced by the density of states in the silicon source/drain electrodes in contrast to the metallic electrodes assumed for other SET compact models. Furthermore, the electric field around the QD modifies the wave function shape, which influences the tunneling rates and leads to varying peak height and shape. We employ an empirical prefactor for the current peaks in order to account for such effects and to obtain a better

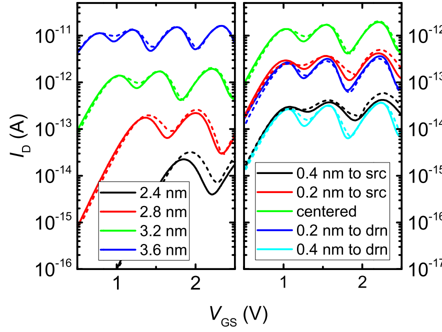


Fig. 2. Comparison between 3-D simulation (dashed) and SPICE simulations (solid) with the SET compact model developed for this article. Left: variations of the QD diameter for a centered dot. Given in the legend are the respective values of $d_{dot}$ (2.4–3.6 nm). Right: variation of the vertical position of the dot for the nominal dot diameter of 3.2 nm. The transfer characteristics are obtained at a $V_d$ of 50 mV and at room temperature.

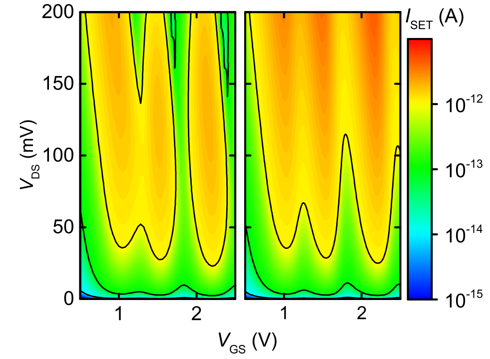


Fig. 3. Stability plots to compare simulations of the nominal SET using 3-D quantum-mechanics-based methods (left) and using SPICE with the compact model developed and calibrated for this article (right).

agreement with 3-D simulations

$$\mathrm{PF} = \frac{1 - d_1 \exp(-d_2 n)}{1 + a_1 \exp(-a_2(0.5 * \tilde{V}_{ds} + \tilde{V}_{gs}))}. \quad (2)$$

The numerator depends on the electron number $n$ and describes the decreasing peak height close to the threshold voltage, as observed in Fig. 2. The denominator modifies the peak shape and depends on the normalized voltages $\tilde{V}_{ds}$ and $\tilde{V}_{gs}$ defined by Inokawa and Takahashi [3]. For the variations considered in this article, we use constants $d_1 = 0.8$, $d_2 = 0.3$, and $a_1 = 0.1$ obtained by fitting the compact model to the 3-D simulations. The peak shape exhibits some dependence on geometry and temperature, $T$, which is approximated by the following expression ($d_{dot}$ and $z_{dot}$ in nm, $T$ in K):

$$a_2 = 4 + 0.3 d_{dot} - 2 \exp(-2 z_{dot}) + \left(\frac{T}{224}\right)^2. \quad (3)$$

Important parameters of the original Inokawa and Takahashi [3] model as well as the modified model used in this article are the tunneling resistances $R_s$ and $R_d$, as well as the capacitances $C_s$, $C_d$, and $C_g$ which couple source (s), drain (d), and gate (d), respectively, with the QD. Our model introduces empirical terms for these parameters, which have been calibrated to a set of 3-D simulations, where we varied geometrical properties as well as external quantities like temperature and voltages. The expressions for the tunneling resistances reflect the exponential dependence of the tunneling currents on QD size and position, while the capacitances change linearly for small geometric variations (all dimensions in nm, capacitances in aF)

$$C_s = 0.19 d_{dot} - 0.317 z_{dot} - 0.228 \quad (4)$$
$$C_d = 0.19 d_{dot} + 0.317 z_{dot} - 0.228 \quad (5)$$
$$C_g = 0.11 d_{dot} - 0.085 t_{gp} - 0.070 \quad (6)$$
$$R_s = 4.23\ T\Omega \cdot 10^{-2.2 d_{dot} + 5.0 z_{dot} + 0.001 T} \quad (7)$$
$$R_d = 4.23\ T\Omega \cdot 10^{-2.2 d_{dot} - 5.0 z_{dot} + 0.001 T}. \quad (8)$$

The parameters in (2)–(8) are of empirical nature, and their values were determined by simultaneous fitting of the device characteristics for different geometries and temperatures. Finally, we obtain an empirical model that explicitly includes QD size and position, as well as the gate-to-pillar distance as model parameters, in addition to temperature and the external potentials. Fig. 2 illustrates the agreement of the 3-D simulations with HSPICE simulations using the calibrated compact model. A so-called stability plot is displayed in Fig. 3 and shows the SET current dependence on both drain and gate voltages. It proves the good qualitative agreement between the compact model and 3-D simulations for drain voltages below 100 mV. In this operation regime, the CB dominates the electron transport, and all the tunneling events use the ground state of the QD. For higher drain bias, the carriers can overcome the CB and tunnel additionally through QD energy states above the ground state. This regime is not well described by the compact model. However, it is also less suitable for possible applications due to the more irregular oscillation peaks when several QD energy states are involved in the tunneling process. It should be noted that the relative error between the compact model and 3-D simulations depends strongly on the point of operation. Peak currents for drain voltages below 100 mV have a maximum relative error of about 10%. Between the current peaks, the relative error increases up to 30% for drain voltages below 50 mV and up to 100% when the drain voltage approaches 100 mV. Considering the variation of the SET characteristics over many orders of magnitude when varying dot size or position we consider this still a suitable agreement between compact model and 3-D simulations for a variability study, For better quantitative agreement a model with more physical background would be instrumental that captures the dependence of the tunneling current on QD properties and bias voltages more natural compared to the empirical calibration provided here. However, the derivation of a completely new model from basic physical principles would be clearly beyond the scope of this article, focusing on SET variability.

The SET-FET combinations studied in this article employ NW-based FET devices simulated by using BSIM models [18], at nominal dimensions of 40 nm of diameter (D) and 30-nm channel length ($L_{channel}$). Note that we have previously analyzed the influence of FET parameters on the SET-FET circuit [12]. Fig. 4 shows the amplification effect in a hybrid SET-FET circuit. The small current at the SET terminal is amplified at the hybrid circuit output. The inset of Fig. 4 presents the schematic of a hybrid SET-FET circuit,

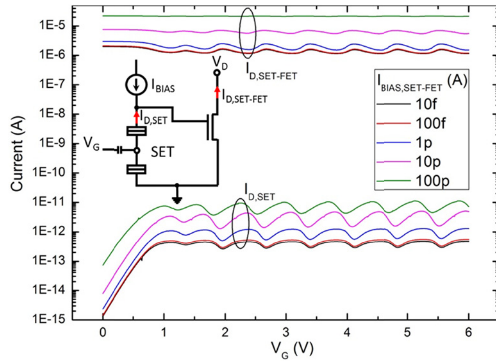


Fig. 4. $I_{d,SET}$ and $I_{d,SET\text{-}FET}$ currents of an NW-based hybrid SET-FET circuit. Inset: schematic of the hybrid SET-FET circuit.

including a current source ($I_{BIAS}$) and a voltage source ($V_d$) [2]. Two different parameters have been used to characterize its performance: 1) the output drive current ($I_{d,SET-FET}$) and 2) the CB oscillations amplitude along the simulated period, expressed by the $h_{ID}$ parameter ($h_{ID} = I_{d,max}/I_{d,min}$), which describes the contribution of the SET into the whole hybrid circuit current. The amplitude $h_{ID}$ has special importance as most proposed SET applications make use of the CB oscillations to implement functionality like logic gates or memory cells [1]. For such scenarios, $h_{ID}$ has a relevance to SETs comparable to the on/off ratio for MOSFETs. Hence, a high value for $h_{ID}$ of at least 10 would be desirable. The period of the CB oscillations determines the gate voltage range necessary to switch circuits based on SETs. For keeping power consumption low, the oscillation period should be as low as possible. We discuss influences on this additional parameter to some extent in Section III.

An important building block of the circuit is the current source [Fig. 4 (inset)]. This element generates a voltage difference between gate and source terminals to switch-on the FET, which operates in the subthreshold region. Fig. 4 also shows the influence of the different values of $I_{BIAS}$ on the output characteristic of the circuit. In the following, we set $I_{BIAS}$ to a value of 10 pA. It should be noted that the SET drain voltage might exceed 100 mV when the SET in the SET-FET circuit operates in the off-regime. Thus, the characteristics displayed in Fig. 4 are not well described for $V_{gs} < 1$ V due to the limitations of the SET compact model for high drain voltages. In the following, we will evaluate the SET-FET characteristics only in the oscillating regime where the SET model operates within its specifications.

### B. Variability Influence on the SET-FET Performance

The need for a high integration level of the electronic devices pushes their dimensions to scale down toward the nanometer regime. In this context, when the dimensions go under a few tens of nanometers device variability arises as the most detrimental factor that leads to a relevant device reliability reduction. To determine their influence on the hybrid SET-FET circuit behavior, we have considered two different cases: 1) the individual impact of each QD characteristics and $V_{T,FET}$ variation and 2) the impact of the external parameters ($I_{BIAS}$, $V_d$, and $T$). The 10 000 sample Monte Carlo analyses were carried out per parameter change. The impact of variability was modeled by using the corresponding FET parameters into BSIM models, and in the case of the SETs as a shift of the different QD design parameters ($z_{dot}$, $d_{dot}$, and $t_{gp}$). The process variation level is arbitrarily defined at a 10% shift of all SET and FET parameters. The variability impact has been evaluated using a statistical distribution with mean ($\mu$) and standard deviation ($\sigma$) parameters, obtaining the device variation ratio $3\sigma/\mu$ (%).

## III. Impact of QD Variations on SET-FET Circuits

QD characteristics deviate from the ideal characteristics due to the difficulty to ensure the optimal dimensions, enhanced by the small dimensionality of the system. Then, to simulate the impact of the variations of QD characteristics on single SETs and on hybrid SET-FET circuits is of high interest. All the simulations consider room temperature operation.

### A. Relevance of QD Variations in Single SET Behavior

First, we have studied the impact of the variation of QD characteristics on a single SET. Fig. 5 shows the $I_{D,SET} - V_G$ characteristics when $z_{dot}$ [Fig. 5(a)], $d_{dot}$ [Fig. 5(b)], and $t_{gp}$ [Fig. 5(c)] are varied. Regarding the variation of the QD position within the oxide layer, Fig. 5(a) presents the maximum SET output current when the QD is centered. The thickest tunneling barrier always dominates the current flow due to the exponential dependence of the tunneling current on the barrier thickness. Thus, the center position leads to maximum current. Larger $I_{D,SET}$ shift is obtained when the QD is closer to drain than to source terminal (53× and 46×, respectively), which could be explained by the asymmetry of the electrostatic potential between source and drain due to the applied drain bias. In the case of the oscillation amplitude $h_{ID}$, we find a continuous increase in the relation between maximum and minimum of $I_{d,SET}$.

The largest range of current variation (400×) is observed when the QD size is varied. Fig. 5(b) indicates that the maximum current is achieved when the QD size is larger, which is related to the smaller tunnel junction values as the distance between QD to S/D terminals gets smaller. In the case of the $h_{ID}$, we observe a continuous reduction of this relation as the $d_{dot}$ increases. Regarding the gate-to-pillar ($t_{gp}$) variation, Fig. 5(c) shows a negligible variation of $I_{d,SET}$ and $h_{ID}$ (not shown to avoid redundant data). This behavior is related to the fact that this parameter mainly affects the SET gate capacitance, which in turn, does not influence $I_{d,SET}$, but it presents more relevance (15%) on the CB oscillations period, as this depends on $e/C_g$ [19].

### B. Influence of QD Variations on SET-FET Circuit

As it has been already stated, the goal of the SET-FET circuit is to amplify the low current level provided by the single-electron device ($I_{d,SET}$). Hence, some additional building blocks are required, e.g., $I_{BIAS}$ and $V_d$. Fig. 6 depicts the influence of the QD characteristics on the hybrid SET-FET circuit. Regarding the QD location [Fig. 6(a)] within the

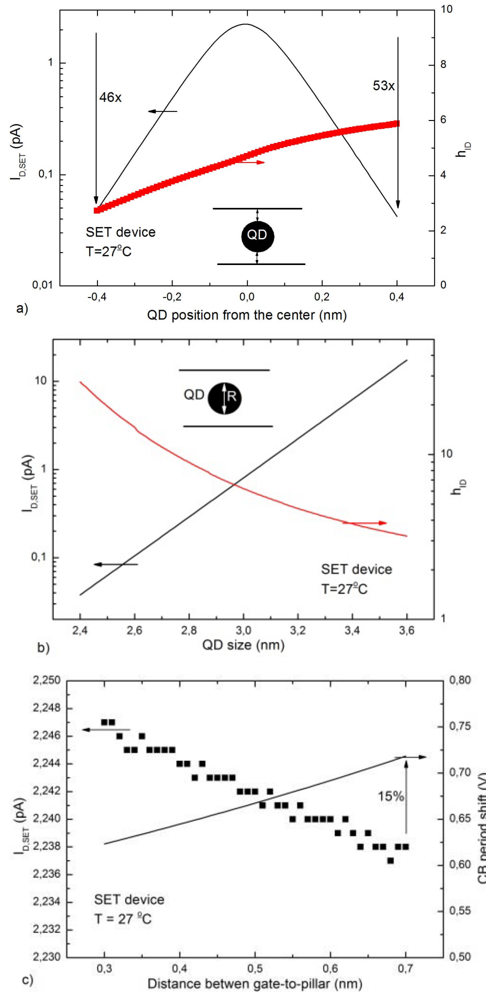


Fig. 5. Influence of the QD position, i.e., (a) $z_{dot}$, (b) $d_{dot}$, and (c) $t_{gp}$, into the behavior of a single SET. The nominal values of the QD characteristic of our SET is $z_{dot} = 0.0$ nm, $d_{dot} = 3.2$ nm, and $t_{gp} = 0.7$ nm.

$SiO_2$ layer, the minimum current occurs when the QD is at the center of the oxide layer. This behavior is not intuitive as it does not reproduce the single performance of a single SET (Fig. 5). It is related to the use of a constant $I_{BIAS}$; when the QD has shifted away from the center, $V_{d,SET}$ increases in order to compensate for the higher tunneling resistance [Fig. 6(d)], increasing $V_{g,FET}$, and hence, the FET current. In the case of the $h_{ID}$ analysis, we obtain the same behavior; the minimum value is at the central QD position.

For the case of the variation of QD size, Fig. 6(b) presents the minimum $I_{d,SET-FET}$ value for the largest QD size. The aforementioned explanation is valid for this case as well. In the case of the $h_{ID}$ parameter, the minimum value is observed at the maximum QD size. Finally, Fig. 6(c) shows a negligible influence of the gate-to-pillar distance on the output current, but more relevant variation (13%) of the CB oscillations period is observed. Note that in Fig. 6(d) larger $V_{d,SET}$ is obtained when the QD is shifted to the drain region.

### *C. Enhancement of the SET-FET Circuit Output Current*

The CB effect is only observable for SET drain voltages below a limit given by $e/C_{\Sigma}$, where $C_{\Sigma}$ is the total

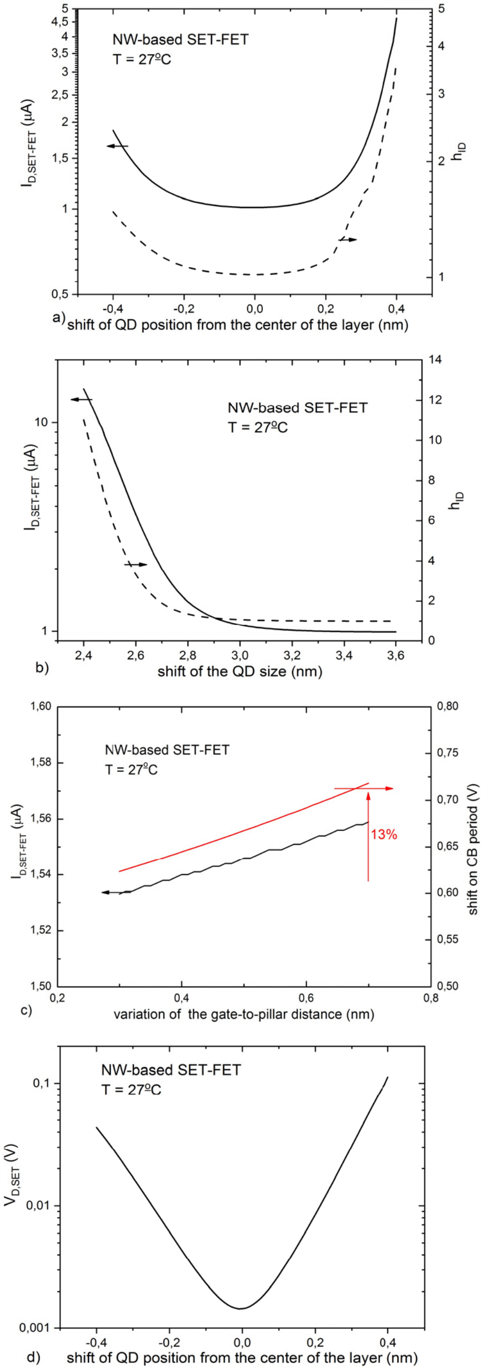


Fig. 6. QD position impact, i.e., (a) $z_{dot}$, (b) $d_{dot}$, and (c) $t_{gp}$, into the performance of a SET-FET circuit. (d) $V_{d,SET}$ evolution when QD position shifts away from the oxide layer center.

QD capacitance. For our devices, $C_{\Sigma}$ is in the range of 1 aF, thus SET drain voltages must be around 100 mV or below. As a consequence, the FET operates at a low subthreshold level, which affects the hybrid circuit performance. This section describes a mitigation method in order to improve the SET-FET performance by enhancement of the output current.

Note that, $C_{\Sigma}$ and $V_{T,FET}$ are usually defined by the fabrication process and are not easily modified. We propose a modified SET-FET circuit, which is depicted in the inset of Fig. 7(a). By introducing an additional voltage source at the source terminal of the FET the effective $V_{T,FET}$ will

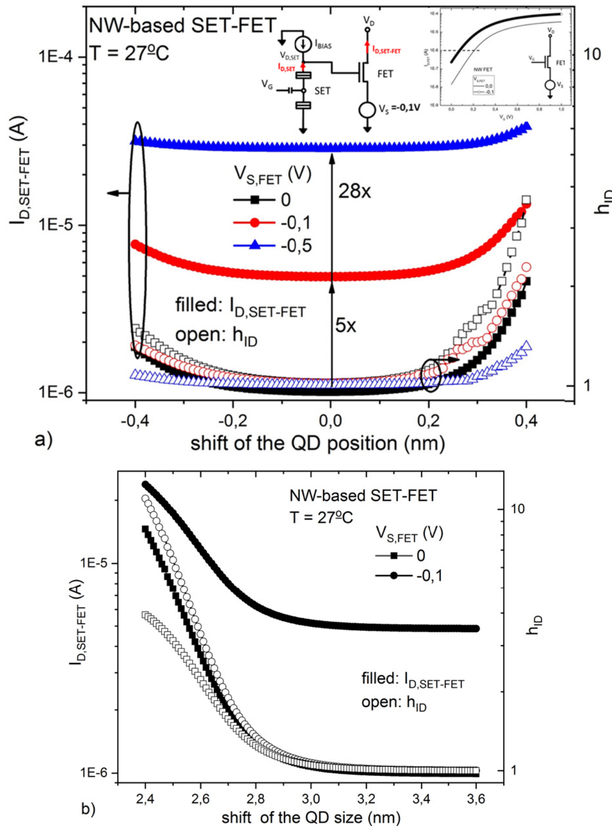


Fig. 7. Performance of a SET-FET circuit when an additional $V_{s,FET}$ is applied and the nominal QD characteristics are modified, i.e., (a) $z_{dot}$ and (b) $d_{dot}$. The inset presents a new configuration of the hybrid SET-FET circuit to enhance its behavior.

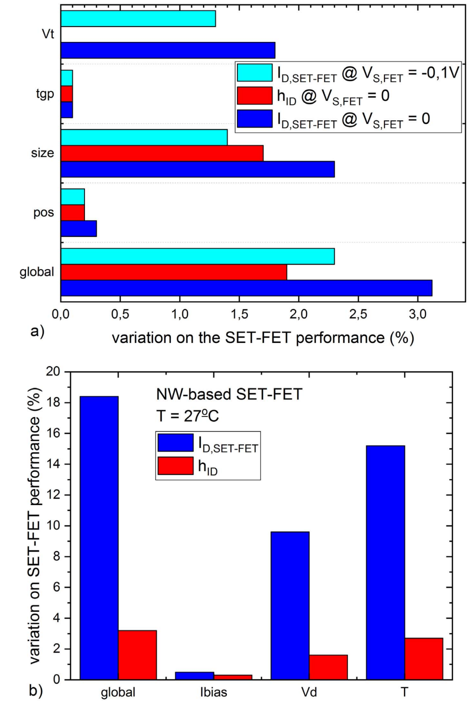


Fig. 8. Impact of the device variability in front of different scenarios at room temperature. (a) When SET characteristics ($z_{dot}$, $d_{dot}$, and $t_{gp}$) and $V_{T,FET}$ are individually considered. (b) Environmental conditions ($I_{BIAS}$, $V_d$, and $T$) and variability contribution are taken into account for the SET-FET behavior.

be reduced. The application of an additional negative voltage at the FET source terminal causes an increase in the output current. In fact, unlike the conventional hybrid SET-FET performance, we can determine that the FET device is now working at a near-threshold level instead of subthreshold, which involves a change on the device regime. Fig. 7 depicts the influence of this change on the SET-FET performance. It is worth noting that a large negative value of $V_{s,FET}$ could entail larger leakage current through the gate of the FET device. If the FET gate leakage gets too high, the bias current will flow through the FET and bypass the SET, deteriorating the SET-FET functionality. Thus, either a very low leakage FET or a sufficiently low level of voltage is recommended. Regarding the behavior of $h_{ID}$, we observe the minimum value when the QD is centered, but an asymmetrical behavior is obtained when the QD shifts to the extreme sides of the layer, becoming significantly more relevant at the drain region. With increasing $V_{s,FET}$ lower $h_{ID}$ values are obtained when the QD is located closer to the drain–source region. Under this new configuration, a relevant increase of the output current is observed (5× and 28×) in the relation of the $V_{s,FET}$ (−0.1 and −0.5 V, respectively). The minimum current is still obtained when the QD is centered within the $SiO_2$ layer. The largest $V_{s,FET}$, the biggest leakage current will appear through the circuit.

On the other hand, Fig. 7(b) shows that the addition of the voltage source affects the circuit performance when the size of the QD is modified. With this new configuration, a larger QD size causes a larger $I_{d,SET-FET}$. With respect to the gate-to-pillar distance, it does not have any relevant influence on the final output current.

## IV. Variability Relevance on SET-FET Behavior

In the previous section, we demonstrated how geometrical variations of QD size and position have a strong impact on the performance of the SET-FET circuit. Additionally, variations on the environmental conditions, e.g., temperature, affect the final circuit behavior. In the following, we compare the impact of these sources of variability in order to determine the most critical factors for reliable circuit operation.

First, we have simulated the variability impact introduced by the devices that compose the hybrid SET-FET circuit. A 10% variation is independently defined to the SET characteristics ($z_{dot}$, $d_{dot}$, and $t_{gp}$) and $V_{T,FET}$ is modeled as mentioned in Section II. Then, the effect of the variation of all parameters simultaneously (global) has been studied, as well. Fig. 8(a) depicts the variation, in percentage, of the output current of the SET-FET. While the highest impact on the hybrid circuit variability comes from the size of the QD, the lowest influence is observed for the distance between the gate and the pillar. Regarding $h_{ID}$ similar results are obtained.

On the other hand, for a complete study of the variability impact on electronic circuits, it is of high relevance the analysis of the influence of the external conditions, e.g., temperature, voltages, and current source. In the case of the SET-FET circuits, temperature influence entails a more relevant impact on the hybrid SET-FET circuit [12], as the SET is highly sensitive to these variations, and additionally,

FET operates at subthreshold level, which makes it weaker against variability. So, in this section, we have solely regarded the influence of the variation of the experimental conditions (i.e., $I_{\mathrm{BIAS}}$, $V_{\mathrm{d}}$, and temperature). Fig. 8(b) shows that temperature is the main source of variability on the hybrid circuit, as it introduces a larger level of variation on the output current. In contrast, $I_{\mathrm{BIAS}}$ introduces the smallest variation level. Regarding the additional voltage source at the source terminal of the FET device, it modifies the hybrid circuit variability level, as well. For this, Fig. 8(a) compares the introduction of this additional voltage source ($V_{\mathrm{s}} = -0.1$ V) on the hybrid circuit variability; a relevant reduction is obtained that could be related with the fact that the level of the output current is larger. This behavioral change can be related to the smaller threshold voltage of the FET, as it is reduced by $V_{\mathrm{s,FET}}$.

## V. Conclusion

The influence of the QD characteristics into SET-based circuits (e.g., hybrid SET-FET circuit) performance has been analyzed. The variation of the QD size ($d_{\mathrm{dot}}$) is the most relevant for a single SET and also for a hybrid circuit. In contrast, the gate-to-pillar distance has presented a negligible impact on the output current, but a more important impact on the CB oscillations period. As QD parameters cannot be modified once manufactured, the introduction of an additional voltage source at the source terminal of the FET device modifies the electrical fields on the circuit and provides better circuit performance, i.e., larger output current. In terms of variability of a SET-FET circuit, the size of QD presents the highest impact on the overall hybrid circuit behavior. When the external conditions ($I_{\mathrm{BIAS}}$, $V_{\mathrm{d}}$, and $T$) are considered as the source of circuit behavioral variation, the operation temperature arises as the most relevant factor.

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