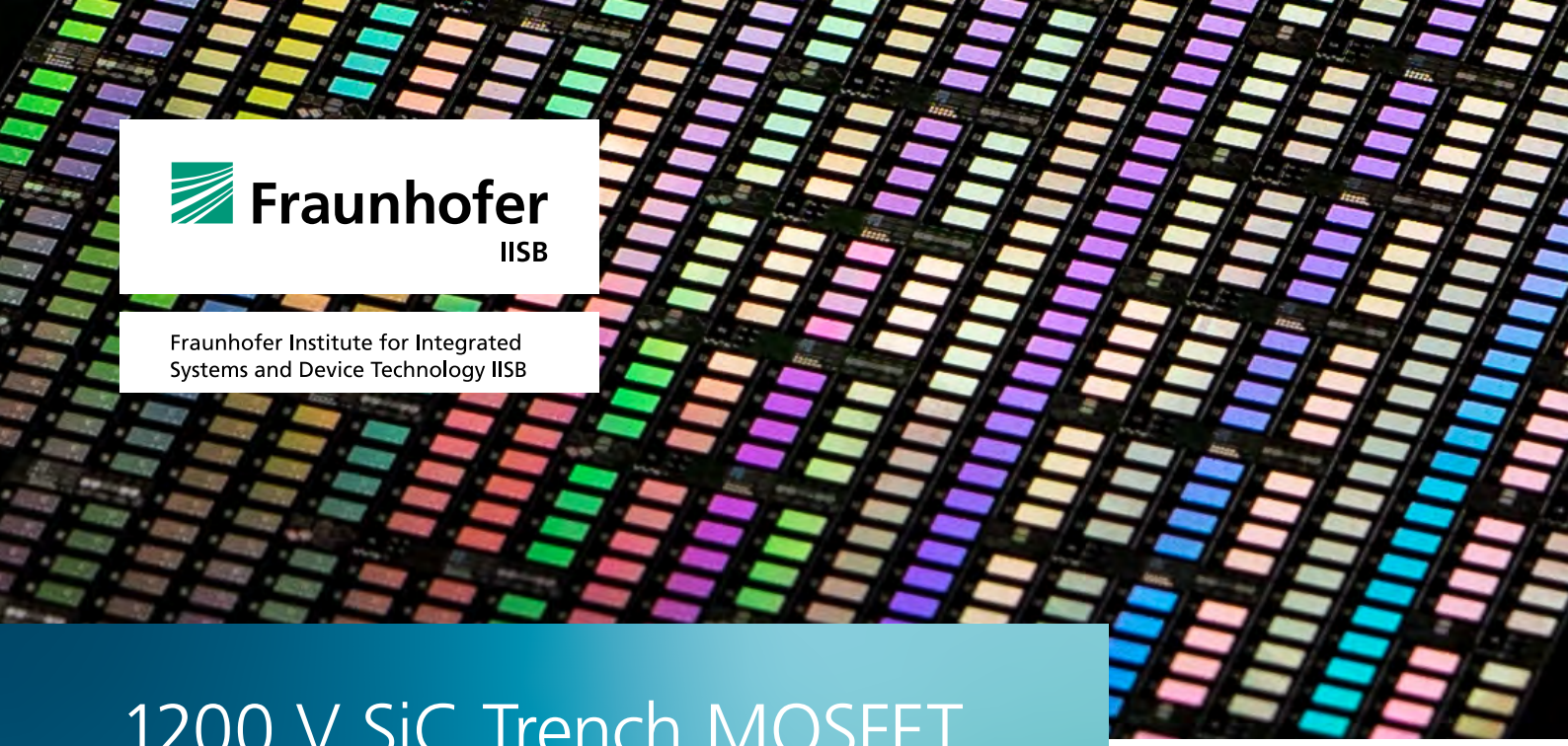

Fraunhofer IISB

Fraunhofer Institute for Integrated Systems and Device Technology IISB

1200 V SiC Trench MOSFET

1200 V SiC TrenchMOS devices on 150 mm 4H-SiC wafer

One approach to further increase the integration density of a Power MOSFET is to introduce a vertical instead of a horizontal channel. The device patterning is realized via trench plasma etching. The reduced cell-pitch of the so-called TrenchMOS due to the absence of a JFET region allows to minimize the chip area and ultimately save chip costs. In addition, the increased channel mobility on the trench sidewall leads to an overall on-resistance ($R_{DS,on}$) reduction compared to Planar MOSFET technology. However, as device architectures becomes more complex, additional manufacturing risks arise. In principle, the n^+-source and p-well regions are implanted in the entire active area. Subsequently, trench structures are formed into this implanted area. Whereas maximal alignment accuracy can be obtained, a drawback of trench-last process is the difficulty to control the etching behavior of the implanted 4H-SiC, which is strongly dependent on the doping concentration. Therefore, the manufacturing process, in which a formation of trenches is followed by implantation (trench-first process), was proposed to form curved trench geometry by a reshape process for reducing high dielectric field concentration at trench bottom corners. Moreover, it is crucial to achieve a high resolution and precise alignment for a mask-compliant structure, which comes with significant lithography system related limitations that impose further high costs. To overcome these challenges, a self-aligned manufacturing process for the formation of the n^+-source and p-well areas, whose alignment is essential for device functionality, was developed at the IISB.

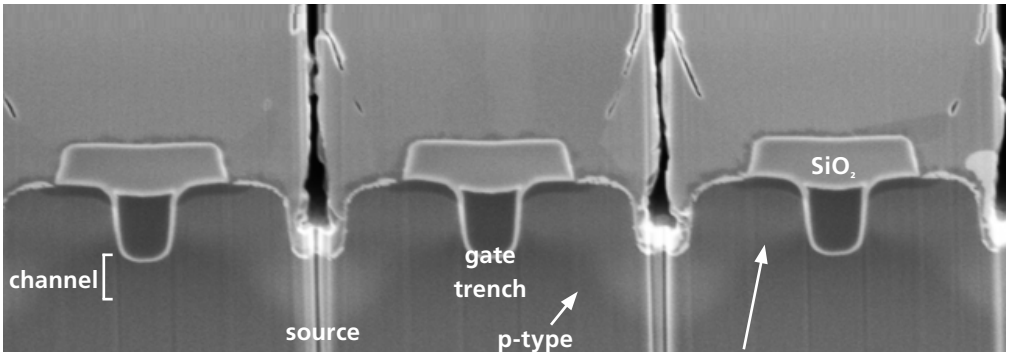

Fig. 1: SEM cross-section image of fabricated SiC TrenchMOS using proprietary trench first technology [1]

[1] Patent pending

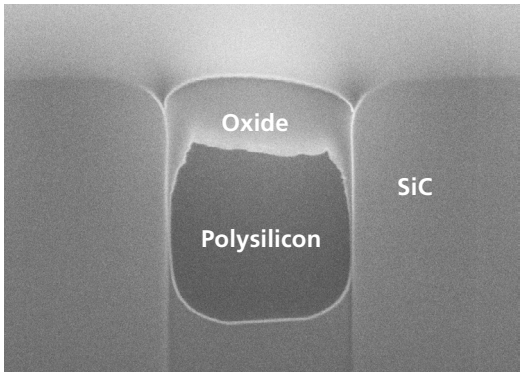

Fig. 2: SEM cross-section image of trench profile prepared via FIB after oxidizing the planarized polysilicon

By oxidizing the previously deposited and planarized polysilicon in the trenches, as depicted in Fig. 2, a self-aligned implantation mask for n^+-source and p-well region is formed that is estimated in advance via process simulator modeling the actual trench shape and oxidized polysilicon. This eliminates the risk of device failure due to misalignment of the corresponding lithography layers. With that, the major benefit here is that implantation for n^+-source and p-well regions within the active area is independent on restrictions regarding the resolution limit and alignment accuracy of the photolithography system. Therefore, the use of a self-aligned process compensates the increased technological effort for TrenchMOS production and simplifies the manufacturing process. Consequently, the production yield increases by minimizing the risk of misalignment of the n^+-source and p-well regions within the active area.

Fig. 3 shows static electrical characteristics in the on- and off-state of the fabricated device shown in Fig. 1, compared with profiles from numerical model and the device simulation. The $R_{DS,on}$ is obtained between 3 and 4 mΩcm² and the device is normally off between 4 and 6 V that can be further improved by design and gate oxide optimization for higher mobility, dielectric breakdown field strength and improved threshold voltage shift. The blocking capability is accomplished up to the target value 1.2 kV that has room for improvement, e.g., a higher shielding effect.

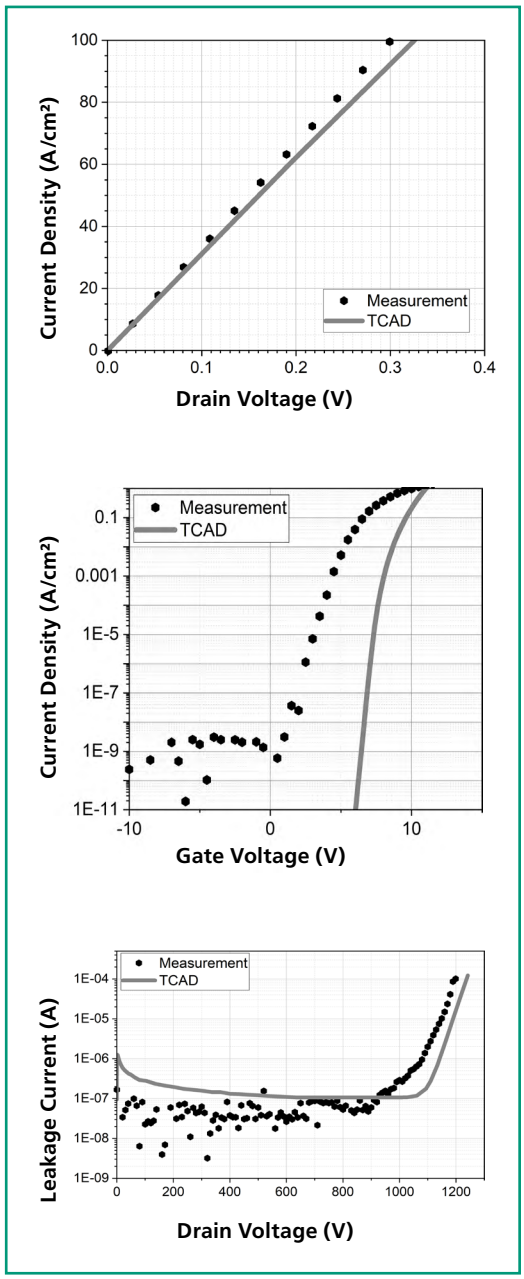

Fig. 3: Output characteristic (top), transfer characteristic (middle) and blocking characteristic (bottom)

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