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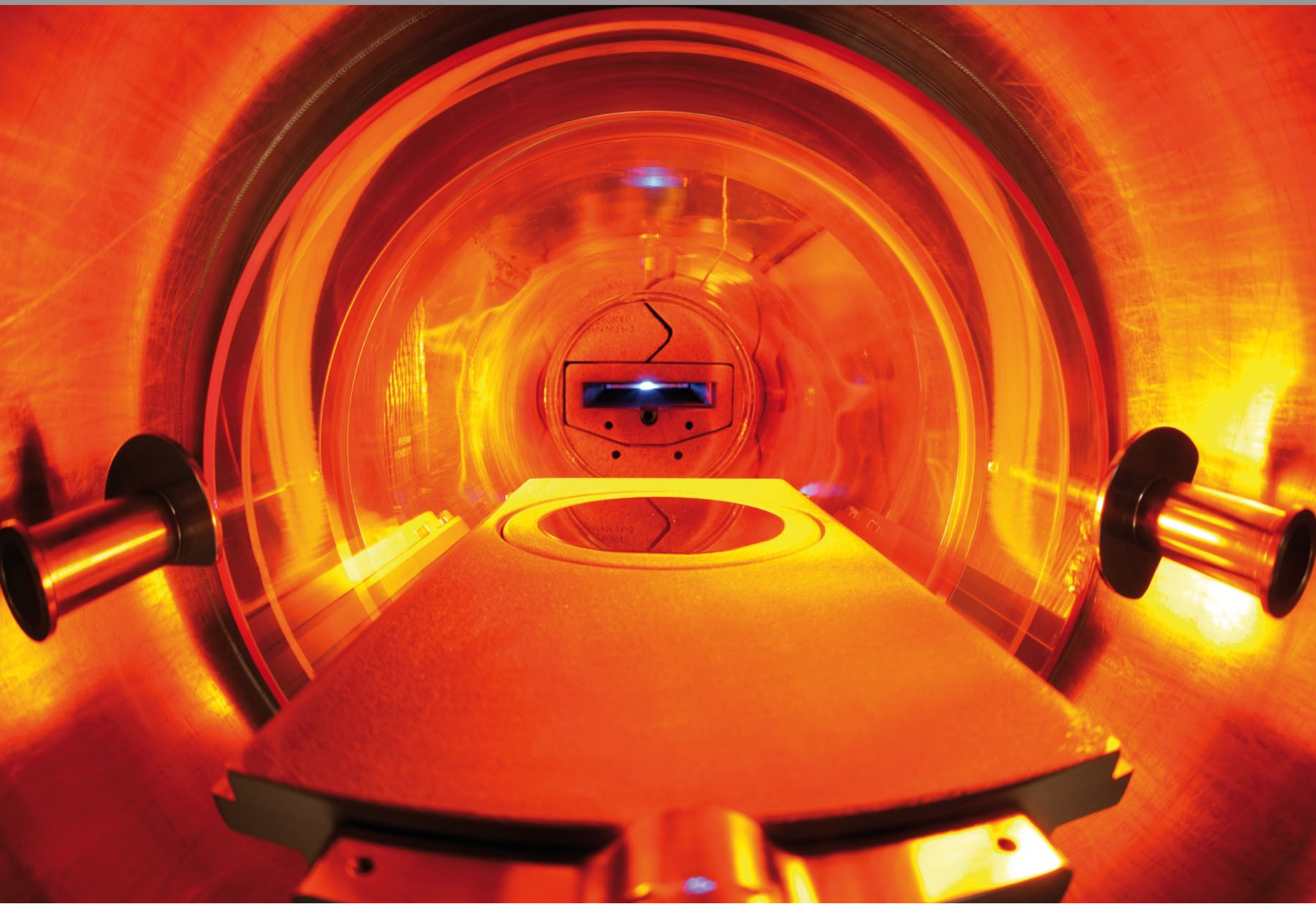
IISB

FRAUNHOFER INSTITUTE FOR INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY IISB



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View into horizontal hot-wall reactor for SiC homoepitaxy during wafer loading. Image: Fraunhofer IISB / Kurt Fuchs

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ACHIEVEMENTS AND RESULTS
ANNUAL REPORT 2011

FRAUNHOFER INSTITUTE FOR

INTEGRATED SYSTEMS AND DEVICE TECHNOLOGY IISB

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PREFACE

2011 has clearly shown that ensuring a safe and reliable energy supply is one of the great challenges of this century. Efficient power electronics will significantly contribute to this goal. Fraunhofer IISB has accepted this challenge and offers solutions in power electronics, semiconductor technology, and advanced materials.

Following our profile "Nanotechnology for Electronics" and "Electronics for Sustainable Energy Use", Fraunhofer IISB conducts applied research and development in close collaboration with industry. This includes semiconductor technology, where IISB is intensifying its research work on wide-band-gap semiconductors. These materials offer major possibilities in energy efficiency applications. Moreover, we are happy to welcome the Infineon Competence Center Silicon Carbide (ICC SiC) at our institute. In semiconductor manufacturing, process control and optimized equipment help saving valuable resources. In that context, IISB acts as a central coordinator of the European research activities on equipment assessment.

In May 2011, the "Energie Campus Nürnberg" (EnCN), a research cluster of university and Fraunhofer institutes from the Nuremberg Metropolitan Region, officially started its collaborative work, representing the regional strength in energy technology. Within the EnCN, IISB has extended its activities in Megawatt power electronics for net applications.

The Fraunhofer Innovation Cluster "Electronics for Sustainable Energy Use", which is coordinated by IISB, successfully passed its interim evaluation. Our series of lectures on power electronics has turned out to be a success story. It has developed into a vivid exchange platform for industrial and academic engineers from the region and beyond. In the first 12 months, this attracted about 800 external engineers and experts.

To strengthen our activities in the field of electric cars, IISB has installed a new research group on "Drives and Mechatronics" and a joint group on "Electric Drive Control" together with the University of Applied Sciences in Nuremberg. In summer 2011, the first phase of the cooperative Fraunhofer system research project on electric mobility (FSEM) was successfully completed. IISB was coordinating the sub-project on "Energy Production, Distribution, and Use" and contributed highly efficient drive units and energy converters for several vehicles.

1

Members of IISB were again awarded with several research prizes, such as the Georg Waeber Innovation Award, the SAOT Student Award, and the Georg Kurlbaum Award. E3Car, a European project with IISB heavily involved, received the Innovation Award 2011 of the ENIAC Joint Undertaking.

1 *Prof. Dr. rer. nat. Lothar Frey, Director of Fraunhofer IISB.*

The last year was a scientifically and economically successful year for Fraunhofer IISB. I would like to thank all colleagues at IISB for their expertise and commitment.

I am happy to express my gratitude to all our public and industrial partners for their fruitful and kind collaboration.

Erlangen, April 2012

Prof. Dr. Lothar Frey

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Brief Portrait

The Fraunhofer Institute for Integrated Systems and Device Technology IISB, founded in 1985, conducts applied research and development in the fields of micro- and nanoelectronics, power electronics, and mechatronics. With its technology, equipment, and material development, its activities in the field of simulation as well as its works on power electronic systems for energy supply and hybrid and electric vehicles, the institute enjoys international attention and recognition.

The headquarters of the IISB is located in Erlangen. Branches of the institute are located in Nuremberg with the Center for Automotive Power Electronics and Mechatronics ZKLM and in Freiberg with the Technology Center Semiconductor Materials THM. The IISB employs about 170 employees. It is one of 60 institutes of the Fraunhofer Gesellschaft and does contract research for industry or public institutions. The institute closly cooperates with the University of Erlangen-Nuremberg.

Scientific Profile

The research and development activities of the Fraunhofer IISB can be summarized in the guiding principles of the institute:

- Nanotechnology for Electronics

and

- Electronics for Sustainable Energy Use

The following topics are comprehensively dealt:

- Nanoelectronics
- Materials for Electronics
- Power Electronics
- Electric Mobility
- Energy Electronics

1 *Building of the Fraunhofer IISB with cleanroom; behind: cleanroom laboratory and building of the Chair of Electron Devices of the University of Erlangen-Nuremberg.*

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Organization and Fields of Activity

The projects and subjects of the Fraunhofer IISB in micro- and nanoelectronics, power electronics, electric mobility, energy supply, and materials research are dealt with interdivisionally in five special departments:

Technology

Here, new materials, devices, and processes from semiconductor technology are developed for CMOS (CLSI, ULSI), nanoelectronics, and power electronics. For that purpose, complete process lines for silicon and silicon carbide are available. In particular, the activities and competences include, inter alia, surface and thin-film technologies for new materials, processes for thin dielectric and metallic layers, ion implantation, circuit modifications and IC repair, nanostructuring, particle electronics, metrology and analysis as well as the development of passive devices.

Semiconductor Manufacturing Equipment and Methods

The focus is put on the development and improvement of new manufacturing equipment and the corresponding methods and processes a ation, process compatibility, contamination, safety, sustainable production, and optimization of resources. Process automation, pre-qualification of equipment, analytics in the IISB analysis laboratory (accredited according to ISO 17025) for micro- and nanotechnology as well as integrated and virtual metrology are possible fields of application.

Technology Simulation

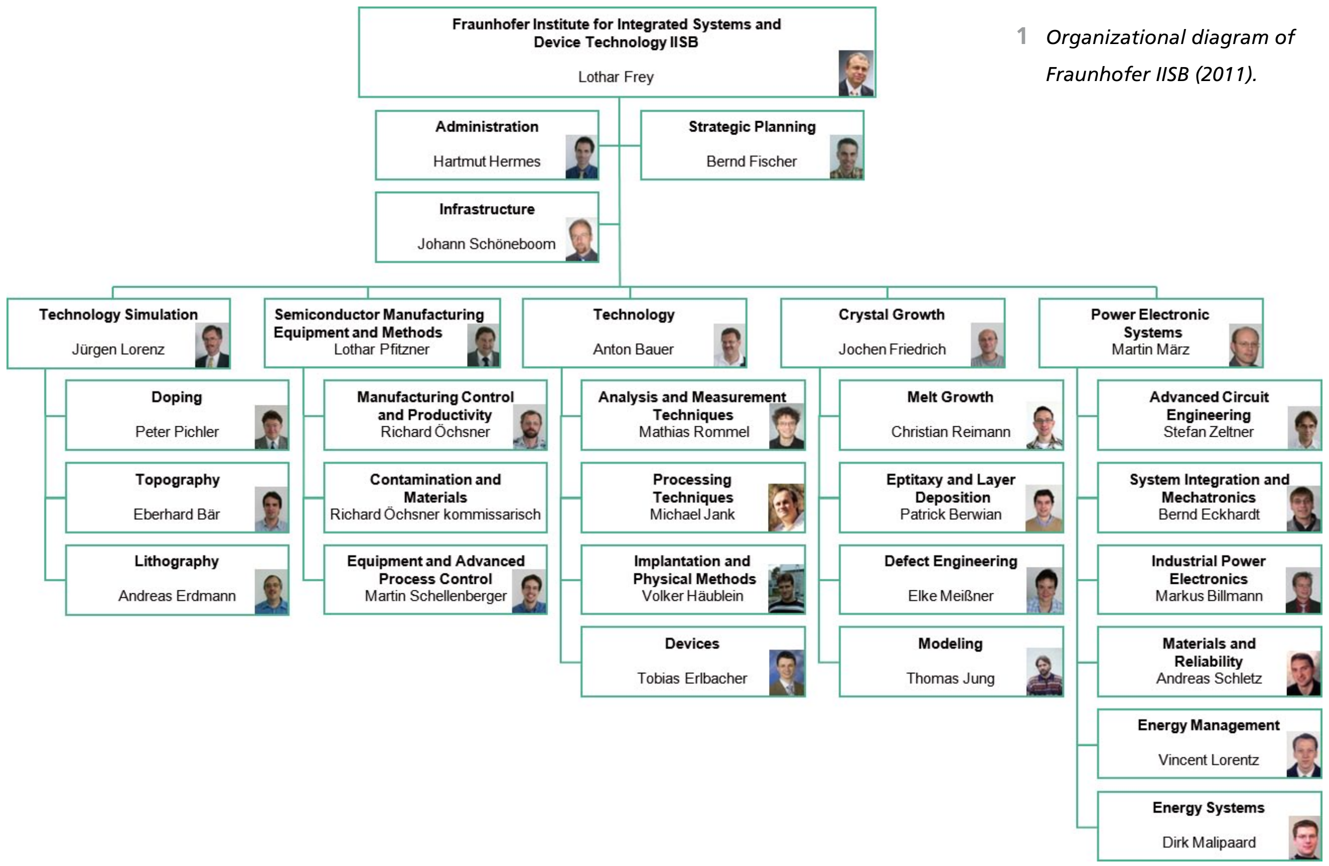
Here, physical models and powerful simulation programs for the optimization of individual processes and process sequences in semiconductor technology are developed and transferred to application. Furthermore, the development of processes, components, and circuits is supported by simulation. Special competence exists in the field of mask design and device development by predictive lithography simulation. Special emphasis is placed on the combination of electric, thermal, and mechanical simulations.

Crystal Growth

The aim is to identify the correlation between the properties of crystalline materials and their growth conditions in order to optimize the industrial process development. For this, experimental and theoretical analyses, metrology, and numerical modelling with software tools specially developed by IISB, represent a strategic alliance. The focus is put on the production of crystal material and crystalline layers for microelectronics, photovoltaics, as well as for optical applications including detector and laser materials.

Power Electronic Systems

The spectrum of the Power Electronic Systems department ranges from the development of new materials reliability testing and error analyses, questions related to circuits and control, packaging and cooling technology, EMC, energy management to the realization of complete system solutions for automotive engineering as well as power supply, systems, and automation engineering. The focus is put on the field of mechatronic system integration, i.e. the integration of power electronics, microelectronics, sensors, and mechanics, electric power converters as well as on technologies for the increase of efficiency and power density in industrial fields of application like electric mobility, power engineering, and network technology.



1 *Organizational diagram of Fraunhofer IISB (2011).*

Fraunhofer IISB in Erlangen

The headquarters of the Fraunhofer IISB is located in Erlangen, right next to the southern campus of the University of Erlangen-Nuremberg. The IISB is provieded with more than 5000 m² of research and development facilities for micro- and nanotechnology, power electronics, and crystal growth. In addition, about 1500 m² high-class cleanroom area are available, which are partly operated together with the University of Erlangen-Nuremberg. With an area of additional 1600 m², an extension building, which will be used mainly for power electronics, will be officially inaugurated in spring 2012. Since summer 2010, the IISB has been operating its new Test Center for Electric Vehicles.

Test Center for Electric Vehicles

Electric vehicles make completely new demands on measurement and test engineering. The Test Center offers a unique infrastructure, customized for these requirements. Single components up to complete vehicles can be measured and optimized. The Test Center includes testbenches for electric drives, energy storage devices, electrical and thermal reliability, and electromagnetic compatibility. Core element is a temperature-controllable roller-type test stand. This test stand can be used to test entire vehicles, e.g., with regard to their range under extreme ambient conditions.

Cleanroom Laboratories

Fraunhofer IISB provides about 500 m² of own cleanroom area and operates the big cleanroom hall of the University (1000 m²) together with the Chair of Electron Devices. Here, research is done on electron devices, processes, materials, equipment development, and metrology for semiconductor technology on silicon, silicon carbide, and nano particles.

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1 *Under construction: extension building of the Fraunhofer IISB in June 2011.*

Center for Automotive Power Electronics and Mechatronics ZKLM

The Center for Automotive Power Electronics and Mechatronics ZKLM is a branch lab of the Fraunhofer IISB located in the "Energy Technology Center" (German abbr.: etz) in Nuremberg. The ZKLM is part of the "Power Electronics Systems" department of the IISB.

In the focus of the research and development work at the ZKLM are power electronic system components for next generation vehicles like two-wheelers, cars, buses, trucks, and airplanes. New technical solutions for electric mobility are developed based on innovations in the field of power electronics, particularly for all kind of electric drives, on-board electrical energy management, vehicle-to-grid systems, and electrical energy storages.

About 680 m² office and laboratory area including a "electric vehicle manufactory" are available for the meanwhile more than 20 engineers and technicians. Besides to test vehicles, the ZKLM uses a proprietary hybrid development platform based on an Audi TT. The engineers use these vehicles for the demonstration, prooftesting, and optimization of system components.

Since 2007, the ZKLM is also domicile of the "Materials and Reliability" and "Industrial Power Electronics" groups. The first one is working on new materials as well as on reliability, lifetime, and robustness issues of power electronic systems in the context of individual application requirements and mission profiles. The group "Industrial Power Electronics" develops components for the power engineering (mega watt power electronics).

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Content

1 *Stuff of the ZKLM (Center for Automotive Electronics and Mechatronics) in Nuremberg with hybrid and electric vehicles.*

Content

Technology Center for Semiconductor Materials THM

The branch lab of IISB in Freiberg, the Fraunhofer Technology Center of Semiconductor Materials (THM) is organized as a joint department of the Fraunhofer Institute for Integrated Systems and Device Technology IISB, Erlangen, and the Fraunhofer Institute for Solar Energy Systems ISE, Freiburg.

THM supports industry in their developments of technologies for the production of innovative semiconductor materials to be used in micro- and optoelectronics as well as in photovoltaics.

The focal areas of research, which are investigated by THM in close collaboration with the Technical University Bergakademie Freiberg, are the production of semiconductor substrates at reduced costs, the improvement of the material quality of crystalline silicon, and III-V compound semiconductors as well as the production of new materials.

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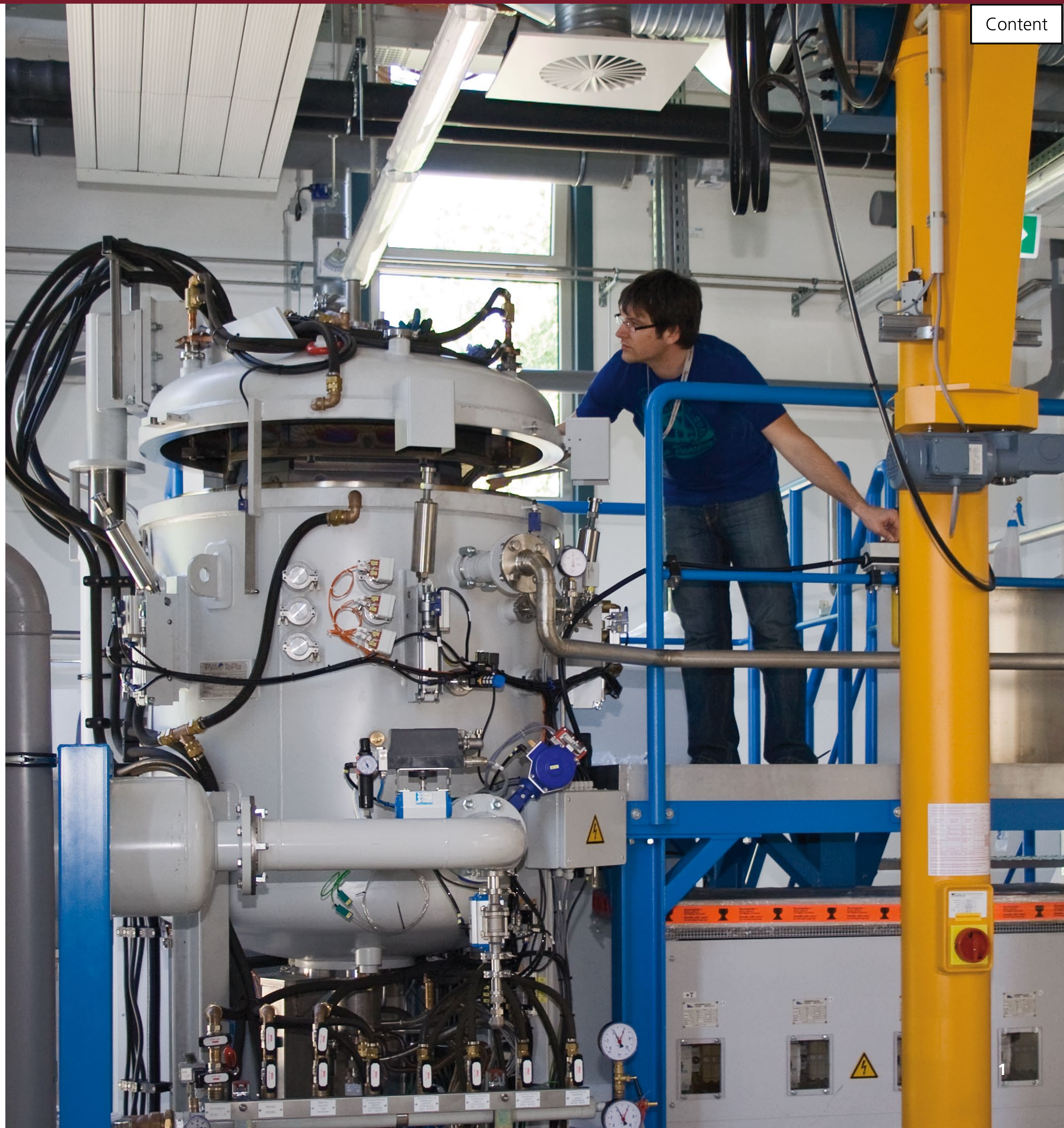

1 *Crystal growth furnace for silicon at the Fraunhofer THM (Technology Center for Semiconductor Materials) in Freiberg, Saxony.*

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Cooperation with the Chair of Electron Devices, University of Erlangen-Nuremberg

IISB and the Chair of Electron Devices (German abbreviation: LEB) of the University of Erlangen-Nuremberg are both headed by Prof. Lothar Frey. Within the framework of a cooperation agreement, the two institutions not only jointly operate the University's cleanroom hall and other laboratories, but also work closely together with regard to teaching and research.

The cooperation of the Chair of Electron Devices and the Fraunhofer IISB allows to cover the entire chain of topics from basic research to the transfer to industry, e.g., in the fields of new dielectrics, metal gates, silicon carbide, and printable electronics. For many years, the vocational training as a "microtechnologist" has been offered jointly by IISB and the Chair of Electron Devices. Employees of IISB assist in courses and internships at the University.

Thus, the following staff members of Fraunhofer IISB regularly give lectures at the University of Erlangen-Nuremberg:

Dr. Andreas Erdmann
Optical Lithography: Technology, Physical Effects, and Modelling

Dr. Tobias Erlbacher
Semiconductor Power Devices

Dr. Michael Jank
Nanoelectronics,
Introduction to Printable Electronics

Dr. Jürgen Lorenz
Process and Device Simulation

Dr. Martin März
Automotive Electronics - Power Electronics,
Architecture and Systems Technology for Electric Mobility

Prof. Dr. Lothar Pfitzner
Semiconductor Equipment Technics

Priv.-Doz. Dr. Peter Pichler
Reliability and Failure Analysis of Integrated Circuits

Prof. Dr. Heiner Ryssel
Cleanroom technology

1 *Chair of Electron Devices of the University of Erlangen-Nuremberg: main building and cleanroom laboratory.*

Content

Advisory Board (2011)

IISB is consulted by an Advisory Board, whose members come from industry and research:

Dr. Reinhard Ploß (Chairman of the Advisory Board)
Infineon Technologies AG

Dr. Dietrich Ernst
Förderkreis für die Mikroelektronik e.V.

Prof. Dr. Nikolaus Fiebiger
retired, former president of the University of Erlangen-Nuremberg

Prof. Dr. Reinhard German
Dean of the Faculty of Engineering Sciences of the University of Erlangen-Nuremberg

Thomas Harder
European Center for Power Electronics (ECPE)

MinR Dr. Ulrich Katenkamp
Federal Ministry of Education and Research (BMBF)

Markus Lötzsch
Nuremberg Chamber of Commerce and Industry

Dr. Andreas Mühe
Siltronic AG

MR Dr. Georg Ried
Bavarian Ministry of Economic Affairs, Infrastructure, Transport and Technology

Dr. Martin Schrems
austriamicrosystems AG

Dr. Karl-Heinz Stegemann
SolarWorld Innovations GmbH

Dr. Thomas Stockmeier
SEMIKRON Elektronik GmbH & Co. KG

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Institute-Specific Offers for Contract Research

According to the Fraunhofer model, Fraunhofer IISB finances itself mostly by third-party funds and does applied contract research and development in close cooperation with its partners as contractual partner of industry and public funding authorities. With its activities in micro- and nanotechnology as well as power electronics, the institute offers a wide range of competencies from basic materials and devices, circuits and processes to overall system development. This is complemented by simulation support, the development of manufacturing devices, analysis, and metrology. Last but not least, the cooperation with the University of Erlangen-Nuremberg is one reason why the whole chain from basic research to prototyping and the transfer in industrial realization can be covered. This wide range of services and flexibility are reflected in variety of the possible constellations of contractual cooperation.

The fields of activities of IISB include, inter alia, the following subjects and offers:

Nanoelectronics

Semiconductor Technology

- processing steps and methods for very-large-scale integrated circuits on Si (VLSI, ULSI) (cleanroom class 10, wafer sizes of up to 200 mm, partly 300 mm)
- processing technology for SiC
- analysis and repair of prototypes of electronic components (sensors, power electronic devices, passives)
- devices for micro- and nanoelectronics, microsystems technology, power electronics and high-temperature electronics on Si and SiC
- implantation of dopants at low and high energy
- production of thin dielectric and metallic layers, in particular MOCVD
- nanostructuring (nanoimprint, "Focused Ion Beam")
- printable electronics based on inorganic nanoparticles
- qualification of gases and chemicals
- analytics and metrology (for example: MOS, I(U), C(U), film resistor, mobility, doping profile, Hall effect, REM, TEM, x-ray analysis, line width, thickness, wafer flatness, and wafer warping)

Technology Simulation

- development of physical and chemical models, algorithms and powerful simulation software for industrial and academic users
- 2D/3D device simulation, circuit simulation
- process simulation (ion implantation, diffusion, etching, layer deposition)
- powerful lithography simulation by rigorous modeling (Software Dr. Litho)
- investigation of process fluctuations
- coupled electrical, thermal, mechanical, and metallurgical simulations
- coupling of structure and equipment levels

Semiconductor Manufacturing Equipment and Methods

- development, testing, evaluation, qualification, and optimization of semiconductor manufacturing equipment, production technology
- characterization of equipment, components, and materials
- equipment assessment
- integrated and virtual metrology
- automation, Advanced Process Control, improved process reproducibility
- optimization of yield, throughput, reliability, safety, energy consumption, and resources
- accredited analysis laboratory for micro- and nanotechnology (DIN EN ISO/IEC 17025:2005)
- contamination analytics: trace impurities on semiconductor and photovoltaic substrates, in process chemicals, process gases, and clean room environments (TXRF, AAS, ICP-MS, GCMS, FTIR, VPD-AAS)
- 450 mm manufacturing
- quality management

Power Electronics

The IISB develops power electric systems for industrial plants, households, electric mobility, as well as for power engineering and network technology. Here, our aim is to make power electronics more efficient, cost-effective, robust, compact, and system-integrateable. This covers a wide range of competencies and applications:

- power conversion
- system integration, mechatronics, system design
- circuit design and simulation, innovative topologies
- smart power ASIC design
- embedded software

Content

Continuation: Institute-Specific Offers for Contract Research

- circuit and control technology
- thermal management, thermomechanical simulations
- energy efficiency, highest efficiency, highest power density
- energy management
- passive devices
- new materials
- packaging
- construction, simulation
- reliability tests and error analysis
- product-related and lifetime-optimizing engineering
- examples for fields of application: frequency converters, electric drives, automation, automotive engineering, high-performance converters, energy storage devices, energy supply, HVDC, local DC networks, photovoltaics, power supply units, and consumer electronics

Electric Mobility

For more than ten years now, electric mobility has been one of the main focuses of the department of power electronic systems at IISB. With many years of experience, we work together with our partners on the following themes:

- considering the overall system power electronic systems for drives, energy storage devices and board supply networks of electric and hybrid vehicles, especially frequency converters, power converters, storage monitoring, and energy management
- charging stations and systems for grid connection for electric and hybrid vehicles
- space-adapted mechatronic system integration
- development and testing of components and vehicles at the IISB Test Center for Electric Vehicles (test benches for drives, batteries, complete vehicles and EMC)

Energy Electronics

Power electronics is an essential enabler of our future electrical energy supply with a large share of renewable energy sources. Among others, IISB is dealing with the following topics:

- megawatt power electronics
- local dc networks
- electrical energy storages in the power grid
- interfaces between the power grid and mobile systems

Materials for Electronics

High-quality materials with customized properties enable increasing efficiency, reliability, and new functionalities. The IISB is a specialist in:

- ultra-thin layers for nanoelectronics (dielectrics, metal electrodes, methods: MOCVD, ALD, PVD)
- inorganic nanoparticles for printable electronics
- materials for power electronics (SiC, magnetic materials, interconnect materials, sintering techniques, reliability tests)
- simulation and characterization of material properties

Crystal Growth

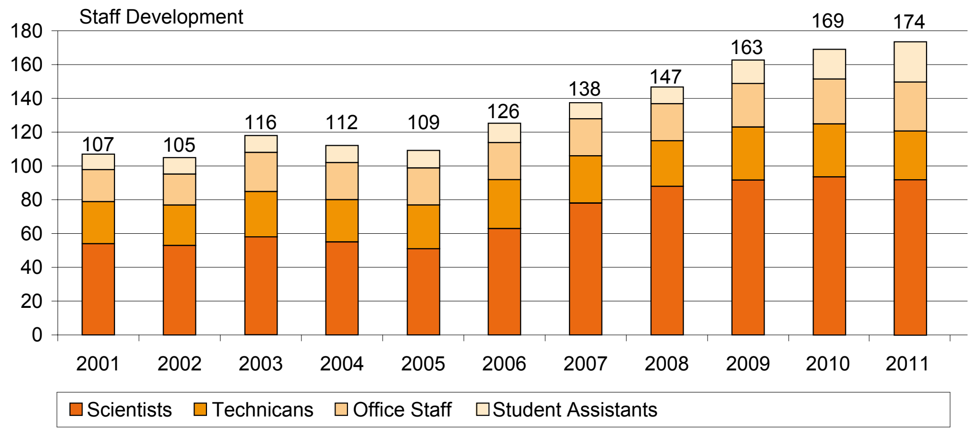
- development and optimization of processes and equipment for bulk growth and epitaxy
- optimized mono- and multi-crystalline silicon for microelectronics and photovoltaics
- wide-band-group semiconductors (SiC, GaN) for optoelectronics and power electronics
- compound semi-conductors
- optical crystals (oxides, fluorides)
- detector and laser crystals for medicine, safety and security
- characterization and metrology
- defect engineering
- numerical modeling, software development (CrysMAS)

The close cooperation with the University of Erlangen-Nuremberg enables the synergetic use and operation of joint research laboratories, coordination of the research activities and application-oriented education and teaching. The broad scientific basis of the IISB is shown also by its membership in networks of the Fraunhofer Group for Microelectronics as well as of the Fraunhofer Energy and Nanotechnology Alliances, the relation to numerous regional, national, and international associations and committees as well as by the cooperation with universities, research institutes, and organizations in Germany, in European countries as wells as, for example, in the United States, Japan, China, India, and Russia.

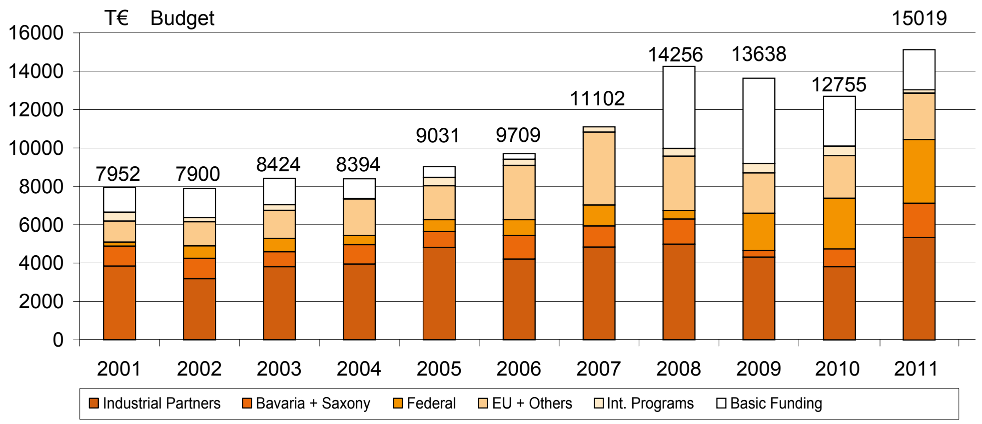
REPRESENTATIVE FIGURES

Content

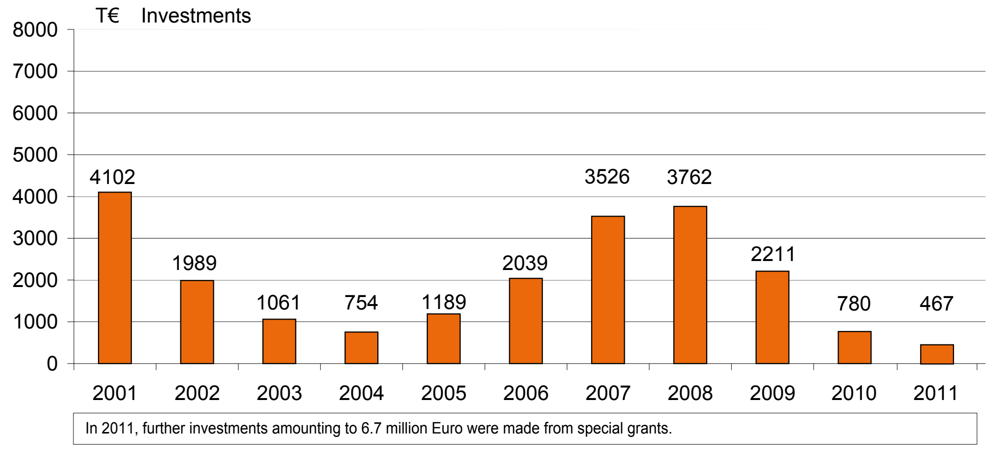
Staff Development, Budget, and Investments



1 *Staff development*
2001 - 2011.



2 *Operating budget according*
to financing domains
2001 - 2011.



3 *Capital investment*
(without basic equipment
and special funds)
2001 - 2011.

FRAUNHOFER-GESELLSCHAFT AND "FÖRDERKREIS"

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The Fraunhofer-Gesellschaft

Research of practical utility lies at the heart of all activities pursued by the Fraunhofer-Gesellschaft. Founded in 1949, the research organization undertakes applied research that drives economic development and serves the wider benefit of society. Its services are solicited by customers and contractual partners in industry, the service sector and public administration.

At present, the Fraunhofer-Gesellschaft maintains more than 80 research units in Germany, including 60 Fraunhofer Institutes. The majority of the more than 20,000 staff are qualified scientists and engineers, who work with an annual research budget of €1.8 billion. Of this sum, more than €1.5 billion is generated through contract research. More than 70 percent of the Fraunhofer-Gesellschaft's contract research revenue is derived from contracts with industry and from publicly financed research projects. Almost 30 percent is contributed by the German federal and Länder governments in the form of base funding, enabling the institutes to work ahead on solutions to problems that will not become acutely relevant to industry and society until five or ten years from now.

Affiliated international research centers and representative offices provide contact with the regions of greatest importance to present and future scientific progress and economic development.

With its clearly defined mission of application-oriented research and its focus on key technologies of relevance to the future, the Fraunhofer-Gesellschaft plays a prominent role in the German and European innovation process. Applied research has a knock-on effect that extends beyond the direct benefits perceived by the customer: Through their research and development work, the Fraunhofer Institutes help to reinforce the competitive strength of the economy in their local region, and throughout Germany and Europe. They do so by promoting innovation, strengthening the technological base, improving the acceptance of new technologies, and helping to train the urgently needed future generation of scientists and engineers.

As an employer, the Fraunhofer-Gesellschaft offers its staff the opportunity to develop the professional and personal skills that will allow them to take up positions of responsibility within their institute, at universities, in industry and in society. Students who choose to work on projects at the Fraunhofer Institutes have excellent prospects of starting and developing a career in industry by virtue of the practical training and experience they have acquired.

The Fraunhofer-Gesellschaft is a recognized non-profit organization that takes its name from Joseph von Fraunhofer (1787–1826), the illustrious Munich researcher, inventor and entrepreneur.

1 *Locations of the Fraunhofer-Gesellschaft in Germany.*

FRAUNHOFER-GESELLSCHAFT AND "FÖRDERKREIS"

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Fraunhofer Groups and Alliances

Fraunhofer IISB is a member of the Fraunhofer Group for Microelectronics as well as of the Fraunhofer Energy and Nanotechnology Alliances.

Fraunhofer Group for Microelectronics

The Fraunhofer Group for Microelectronics VµE has been coordinating the activities of Fraunhofer Institutes working in the fields of microelectronics and microintegration since 1996. Its membership consists of thirteen institutes as full members and three as associated members, with a total workforce of around 2,700 and a combined budget of roughly €307 million. The purpose of the Fraunhofer VµE is to scout for new trends in microelectronics technologies and applications and to integrate them in the strategic planning of the member institutes. It also engages in joint marketing and public relations work.

Further activities of the group concentrate largely on establishing joint focal research groups and projects. In this way, the group is able to provide innovative small and medium-sized enterprises, in particular, with future-oriented research and application-oriented developments that will help them gain a decisive competitive edge.

The core competencies of the member institutes are bundled in the Group's business areas:

- Technology – from CMOS to Smart Systems Integration
- Communication Technologies
- Ambient Assisted Living
- Energy-Efficient Systems and eMobility
- Light
- Safety and Security
- Entertainment

The Business Office of the Fraunhofer Group for Microelectronics based in Berlin serves as central coordination and marketing office. It advises and assists the board of directors of the group on questions regarding strategies, roadmaps, and research coordination.

www.mikroelektronik.fraunhofer.de

Fraunhofer Energy Alliance

The Fraunhofer Energy Alliance is the gateway to the R&D services of the Fraunhofer-Gesellschaft in energy technology and energy economics. In cooperation with partners from industry, the alliance aims at strengthening their technological leadership with regard to energy efficiency and renewable energy sources. The Fraunhofer Energy Alliance offers simplified access to the expertise of the Fraunhofer Institutes particularly to small and medium-sized companies, but also to policy and energy industry.

The Business Areas of the Fraunhofer Energy Alliance are:

- Renewable Energies
- Efficiency Technologies
- Buildings and Components
- Smart Grids
- Energy Storage

www.energie.fraunhofer.de

Fraunhofer Nanotechnology Alliance

The activities of the Fraunhofer Nanotechnology Alliance comprise a wide range of topics such as e.g. multifunctional layers for use in the optical, automotive, and electronics industry. Metallic and oxidic nanoparticles, carbon nanotubes, and nanocomposites are used in actuators, structural materials, and biomedical applications. Moreover, the Fraunhofer Nanotechnology Alliance treats questions regarding toxicology and operational safety when dealing with nanoparticles.

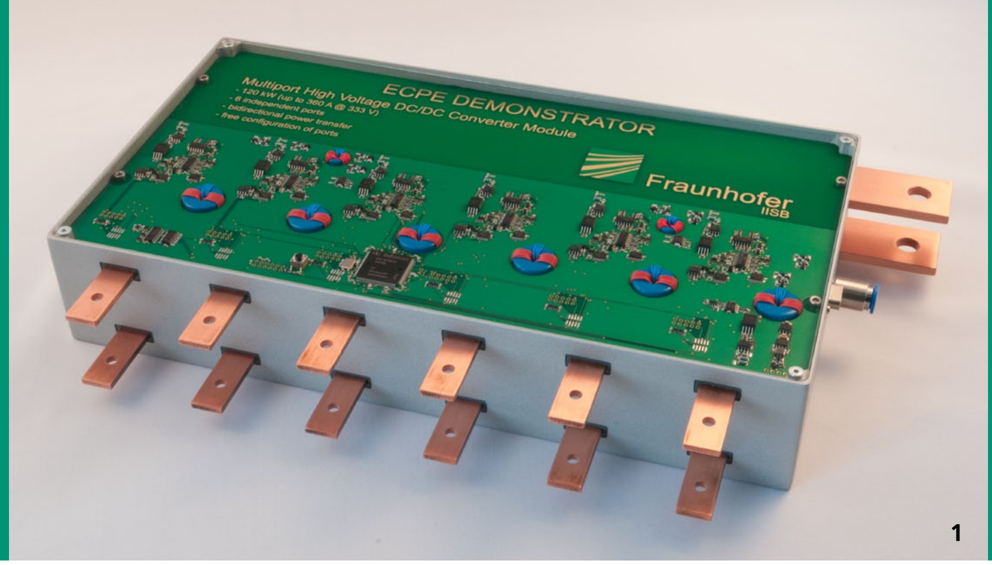
This involves the following Business Areas:

- Nanomaterials and Nanochemistry
- Nanooptics and Nanoelectronics
- Nanobiotechnology
- Nanoprocessing / Handling
- Measuring Methods / Techniques
- Technology Transfer and Consulting

www.nano.fraunhofer.de

1 *SpreePalais in Berlin (Mitte), location of the business office of the Fraunhofer Group for Microelectronics.*

FRAUNHOFER-GESELLSCHAFT AND "FÖRDERKREIS"



1

Content

Innovation Cluster

In 2011, the Fraunhofer Innovation Cluster "Electronics for Sustainable Energy Use" succesfully completed its second year. Coordinated by Fraunhofer IISB, research institutions and companies from the Nuremberg Metropolitan Region combine their expertise in this cooperation network and develop innovative products in the fields of power electronics and power engineering. The objective of the Innovation Cluster is to take up existing unique features of the region in an effective way, to enter new markets and thus to safeguard jobs in the long term.

Electronics for sustainable energy use

Efficient and modern electronics, in particular power electronics, can make an essential contribution to energy saving. Whether in household appliances, consumer electronics or in the office, whether in industrial plants, power supply networks or electric vehicles – potential savings can be found along the entire chain from power generation and power distribution to the end consumer. Due to low-loss components, tailored materials, and intelligent systems, devices, vehicles, and industrial plants are not only less energy-consuming and more efficient, they also become more operationally reliable and compact.

In close cooperation with the existing industrial networks and associations, the Innovation Cluster is intended to realize an even closer coordinated linking between local economy and research. Besides Fraunhofer IISB, research partners of the Innovation Cluster are the University of Erlangen-Nuremberg, the University of Applied Sciences in Nuremberg, the Bavarian Laser Centre and Fraunhofer IIS. The Innovation Cluster also cooperates closely with the "Bayerischer Cluster Leistungselektronik" (Bavarian Cluster for Power Electronics) and the European Center for Power Electronics which is located in Nuremberg. Cluster research is funded by the Bavarian State Ministry of Economic Affairs, Infrastructure, Transport, and Technology and by the Fraunhofer-Gesellschaft within the framework of the "Joint Initiative for Research and Innovation" of the Federal Government as well as by means of orders from industrial partners.

The research activities of the Innovation Cluster comprise the following areas:

- energy-efficiency at work and at home
- smart power grids
- electric mobility

In December 2011, the Innovation Cluster passed its interim evaluation with great success, confirming the funding period until the end of 2012.

Fraunhofer Innovation Clusters

The Innovation Clusters of the Fraunhofer-Gesellschaft are an initiative within the framework of the Federal Government's "Joint Initiative for Research and Innovation". They are regional, application-oriented project clusters between industry and research with a minimum duration of three years. The objective of the Innovation Clusters is to implement interdisciplinary research with scientific excellence in tangible projects. An Innovation Cluster bundles the existing research and development resources and acts as a driver of innovation and as a transfer interface between partners from university to industry. With this initiative, the Fraunhofer-Gesellschaft stimulates the further development of regional centers of excellence and supports the regions' expertise. The project work at the research institutions involved is supported by the Federal Land, industry and the Fraunhofer-Gesellschaft.

www.iisb.fraunhofer.de/innocluster

1 *Developed within the Innovation Cluster: Multiport high voltage DC / DC converter module for smart local power grids.*

FRAUNHOFER-GESELLSCHAFT AND "FÖRDERKREIS"

Content

Förderkreis für die Mikroelektronik e.V.

More than 25 years ago, the founders of the non-profit "Förderkreis für die Mikroelektronik e.V." (development association for microelectronics) recognized the influence and importance of microelectronics in all technical fields and almost all aspects of daily life, with microelectronics as a key technology and innovation motor being decisive for the economic power, jobs, and wealth of a high-tech producing nation like Germany and thus having an essential meaning for a business location.

Therefore, the "Förderkreis für die Mikroelektronik e.V." was launched in 1983 with the goal of promoting microelectronics in and for the region of northern Bavaria. This was made possible by generous donations from industry, large subsidies from the Bavarian government, the permanent support by the IHK Nürnberg für Mittelfranken (the local CCI), as well as by enormous investments by the Fraunhofer-Gesellschaft, and resulted in the start-up of chairs of the Friedrich-Alexander University of Erlangen-Nuremberg and institutes of the Fraunhofer-Gesellschaft (among them the IISB) with ultra-modern equipment.

Besides the industrial members, academic partners of the Förderkreis are the two Fraunhofer institutes IIS and IISB in Erlangen, and of the University of Erlangen-Nuremberg the chairs of Technical Electronics, Reliable Circuits and Systems, Information Technology with Focus on Communication Electronics, as well as the Chair of Electron Devices, which is held by the director of the IISB, Prof. Lothar Frey.

The large activities of the "Förderkreis" include:

- promotion of the cooperation between science and industry
- support of technical and scientific events and presentations
- granting of awards

Especially by the last item, the Förderkreis realizes its goal of promoting research, development, teaching, and technology transfer together with its partners. Thus, in 1996 an innovation award for microelectronics was founded, which is annually granted and endowed with 3000 Euros. Criterion for the jury is mainly an outstanding progress in the field of microelectronics, but also its transfer by a practical utilization by industry. Besides a decoration for special achievements in the field of microelectronics, this award also represents a stimulation for innovative activities and the strengthening of the business location Germany, which depends on ultra-high technology for competing in the world market. The IISB could already provide some of the laureates with Dr. Thomas Falter (1996, together with GeMeTec), Dr. Lothar Frey (1999, together with Nanosensors GmbH), Dr. Andreas Erdmann (2000, together with Sigma-C GmbH), and Marc Hainke, Dr. Thomas Jung, Flaviu Jurma Rotariu, Dr. Matthias Kurz, Dr. Michael Metzger as well as Artur Pusztai (2002), Dr. Martin März and Stefan Zeltner (2005, together with Semikron), Dr. Anton Bauer with Dr. Volker Häublein (2006, together with Infineon), Dr. Mathias Rommel and Holger Schmitt (2008, with Süss MicroTec and S.E.T. SAS) and Dr. Jochen Friedrich (2009, together with SolarWorld Innovations), and Markus Billman and Dirk Malipaard (2011, together with Siemens and Konstruktionsbüro Blösch).

Furthermore, the Förderkreis has recognized the importance of protecting the future of technical education. In this context, in 2000 a youth award endowed with 500 Euro was created in order to support the interests and activities of young people as the future creators of our technical progress. The youth award, which is annually announced in about 300 schools in Bavaria, induces a brisk interest.

Moreover, the Förderkreis supports the stays of guest scientists and graduates at the listed Fraunhofer Institutes and microelectronics chairs.

A support of these activities and promotion goals can be achieved best by a membership in the Förderkreis. Details on this and extended information on the activities of the Förderkreis can be obtained from the contact address below or also from the IISB.

Förderkreis für die Mikroelektronik e.V.
Chief Executive Officer: Dr. sc. techn. h.c. Dietrich Ernst
Office: IHK Nuremberg for Middle Frankonia

Contact
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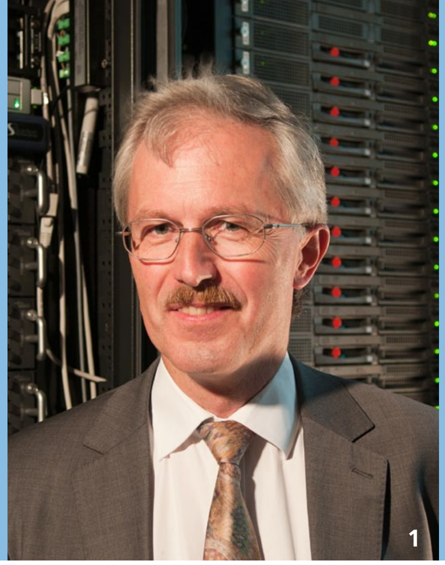
TECHNOLOGY SIMULATION

Focal Areas of Research and Development, Trends, and Potentials

The simulation of semiconductor fabrication processes, devices, and circuits strongly contributes to the reduction of development costs in micro- and nanoelectronics. Among others, this has been confirmed in the International Technology Roadmap for Semiconductors (ITRS), which in its 2011 issue estimated this time and cost reduction at about one third for cases of best practice. The Technology Simulation department contributes to this with the development of physical models and programs for the simulation and optimization of semiconductor fabrication processes and equipment. Furthermore, it supports the development of processes, lithography masks, devices, circuits and systems by providing and applying simulation and optimization tools.

While process and device simulation meanwhile has been largely established in industry as an indispensable tool for the development and optimization of highly scaled devices ("More Moore"), fields like power electronics, photovoltaics, microsystems technology, and the whole domain of "More than Moore" offer a large variety of additional applications. Here, on the one hand, the offer of commercial tools is by far not yet comparable to traditional fields such as the simulation of CMOS transistors. On the other hand, especially these new fields of application often require the combination of heterogeneous competencies, because not only electronic, but also thermal, mechanical, optical, and chemical effects occur. This gives rise to an additional demand for research.

For the Technology Simulation department , this gave rise to both the necessity as well as the opportunity for a systematic extension of its activities to the "More than Moore" sector and the interdisciplinary work required. However, when developing the physical models which are the core of each simulation activity, it inevitably gets obvious that the successful development of simulation for "More than Moore" is not at all possible without solid expertise in simulation for "More Moore". A comparable situation also occurs in industrial production itself: The application of advanced technologies from the "More Moore" sector also leads to improved and more cost-effective products in the "More than Moore" sector. In consequence, as outlined below and reported in a more detail way in two of the following technical contributions, the department has started to work on several new projects in various parts of the "More than Moore" area.



1 *Dr. Jürgen Lorenz, head of the department.*

Content

Some recently finished or newly started projects of the Technology Simulation department highlight the mutual dependence between technologies for advanced scaling and the generation of new applications among others in the "More than Moore" sector: IISB has contributed to the MALS ("Mask Aligner Lithographie Simulation") project funded by the Bavarian Research Foundation. Here, together with the equipment company SUSS, the software house GenISys and the Vorarlberg University of Applied Sciences, models and software for the simulation of mask aligner lithography were developed, based on background work on projection and e-beam lithography. A common aspect for several new projects is the combination of electrical with thermal simulations: In the EU project "ESTRELIA" (Energy Storage with Lowered Cost and Improved Safety and Reliability for Electrical vehicles), the department supports the development of advanced battery management systems by coupled process and device simulations as well as thermal and mechanical simulations. In the CATRENE design project "RELY" (Design for RELIABILITY of SoCs for Applications like Transportation, Medical, and Industrial Automation), it focuses on the combined electrical and thermal simulation of advanced devices for automotive, medical and aeronautical applications where reliability is a key concern. In some new projects directly funded by industry, the department develops and applies models for dopant diffusion for specific applications in photovoltaics and power electronics.

The department will continue its approach to perform focused work on physical models and algorithms in order to develop the necessary skills and tools on the one hand and to transfer these results to industrial applications on the other hand. Here, a close and trustful cooperation based on sharing the work according to the individual competencies and requirements of the partners has been a key element of the success obtained for many years. The overall mission is to extend the well-established and well-proven contributions which simulation offers for aggressively scaled devices in the "More Moore" area to the more diverse requirements and applications which open up in "More than Moore".

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Content

Lithography Simulation in the European EUV Project „EXEPT“

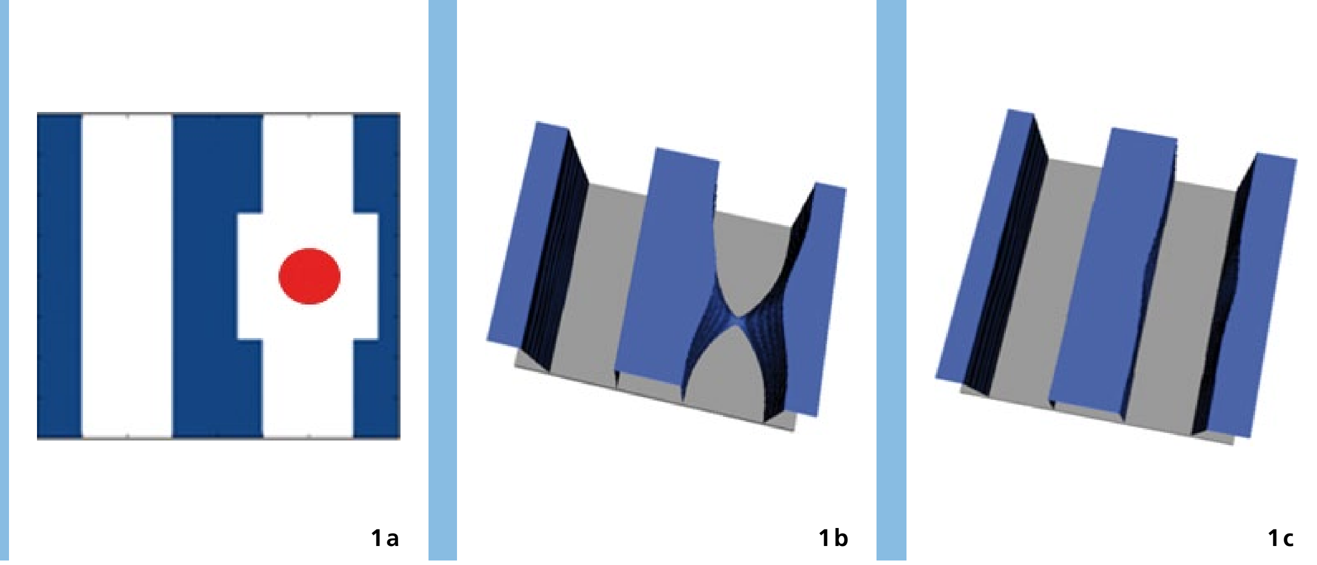
The European project "EXEPT" (**EX**treme UV Lithography **E**ntry **P**oint **T**echnology Development) aims at the development of technologies, tools and infrastructure components required for high volume EUV (**E**xtreme **U**ltra**V**iolet) lithography with 22nm half pitch structures. Companies from the European semiconductor equipment industry, institutes, and a mask shop participate in the project.

The Lithography Simulation group of Fraunhofer IISB supports the technological goals of the project by the development and application of new simulation algorithms for EUV lithography. Main tasks are the development of new models for the resist and mask defect simulation and their application in simulation studies for the project partners. Goal of the resist simulations is to support the selection of photoresists with respect to process stability and line edge roughness. Prior to this, the required resist model calibration was optimized and performed for different resist types with printing and measurement data from the project partners. Goal of the mask defect simulations is a systematic characterization of EUV multilayer defects and the investigation of defect repair strategies. This includes the very challenging extension and optimization of our current defect simulation models in order to deal with the long simulation times and large memory requirements. For an efficient application of the new models, all developments are integrated into the lithography simulator "Dr.LiTHO" of Fraunhofer IISB. In the following, an important extension of the EUV multilayer defect simulation and two typical simulation results will be presented.

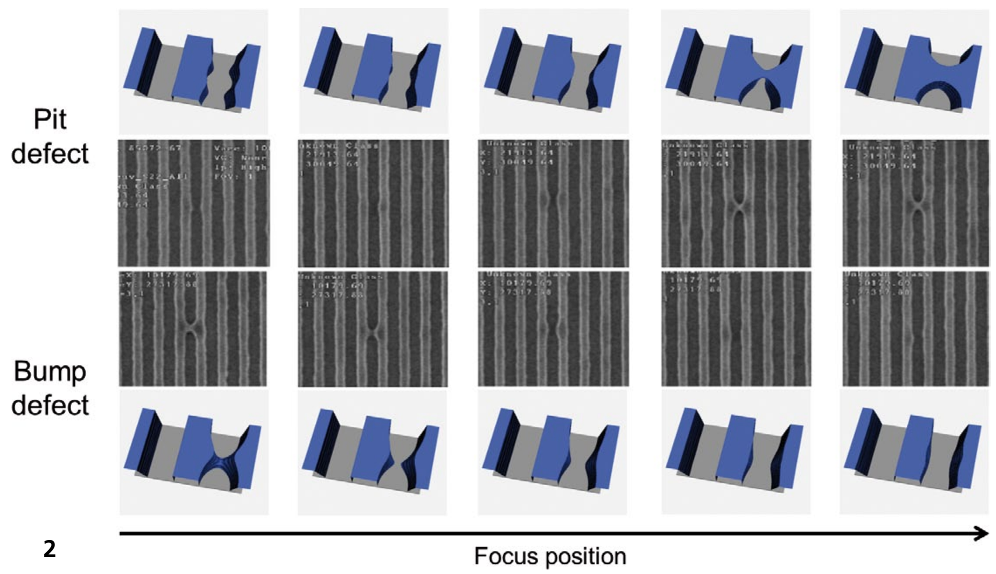
A typical and fully rigorous EUV multilayer defect simulation with "Dr.LiTHO" takes about 24 hours on a state-of-the-art personal computer. This already includes extensive optimizations of all parts of the simulation algorithm. Such long simulation times make the systematic defect investigation and in particular the defect repair investigation very difficult. A powerful solution of the problem is a defect data base approach developed within the framework of the project. The idea of this approach is to split up the mask into the defective multilayer part (EUV multilayer mirror including the defect and the deformation of the whole multilayer structure caused by the defect) as well as the absorber part (lines and spaces, contact holes etc.). The time-consuming computation of the defective multilayer part is performed separately for numerous systematically varied defect parameters and the results are stored in a database. Using the Fraunhofer IISB computer cluster, a significant number of defect simulations can be performed within a reasonable time. Since the simulation time of the absorber part typically is in the range of seconds, this part will be computed on demand during an investigation. The coupling of the flexible absorber simulation with the defect database leads to very fast EUV mask defect simulations with a large parameter range. The simulation time of such a coupled simulation typically is in the range of seconds up to a few minutes. All developed algorithms are evaluated based on experiments and measurement results of the project partners. Using this new simulation model, extensive simulation studies on defect printing and repair are performed.

Figure 1 shows the simulation of an EUV multilayer mask defect repair. The impact of the defect will be compensated by an appropriate rectangular cut-out of the absorbers in the defect vicinity. In order to improve repair and to capture more complex defect shapes, further and more complex cutout geometries are currently being investigated. The described combination of defect database and flexible on-demand mask absorber simulation enables such a complex investigation within a reasonable time frame.

Figure 2 shows the comparison of a printing analysis of real EUV multilayer mask defects and corresponding simulations. The opposite through focus behavior of pit defects (hole in the mask substrate) and bump defects (defective particle on the mask substrate) and the good agreement with the simulations can be seen.



1 *Simulation of EUV multilayer mask defect repair: a) 40nm lines-and-spaces mask with multilayer defect (at the position of the red dot) and with rectangular absorber cut-out for defect compensation, b) resist profiles resulting from the defective mask, c) resist profiles with rectangular absorber cutout.*



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2 *Printing analysis of EUV multilayer mask defects; first and fourth row: simulated impact of pit and bump type defects on the patterning of 40nm lines and spaces with the EUV demo tool; second and third row: corresponding SEM images of experimental wafer prints.*

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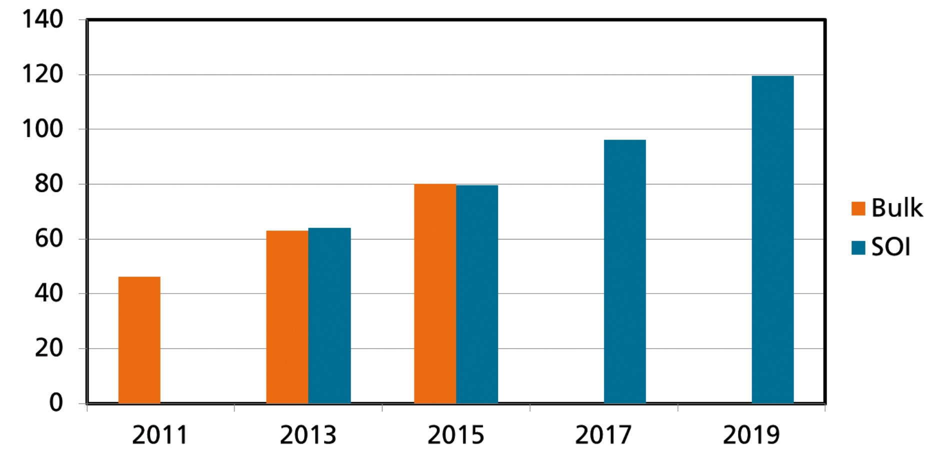
Simulation of Self-heating in Nano-scaled MOSFETs and Thermally Aware Compact Models

The main trend in the development of leading-edge CMOS technologies is the transistor scaling that has enabled a continuous performance improvement of integrated circuits based on these technologies. The International Technology Roadmap for Semiconductors (ITRS) forecasts how CMOS transistors are expected to evolve in future.
According to the ITRS, a transition from bulk silicon transistor architectures to SOI (silicon-on-insulator)-based architectures is expected in the next years. Although both the gate length and the silicon body thickness in the SOI-based CMOS technology are reduced, the on-state current of the transistors should grow with each new generation independently of the transistor architecture. All these trends lead to an increase of the density of the dissipated energy inside the novel transistors. Figure 1 illustrates the resulting increase of the density of dissipated energy in the active regions of transistors for new CMOS generations. The increase of dissipated energy density leads to a significant self-heating of the transistors. The effect of self-heating becomes especially aggravated for SOI-based transistors, because the buried oxide thermally isolates the transistor silicon body from the silicon substrate.

In the European project "THERMINATOR", we investigated the effect of self-heating in MOSFETs envisaged for the next CMOS generations using numerical TCAD simulation. First, the geometrical shape of the transistors and the distribution of the doping impurities in the semiconductor were simulated. Then, electrical current-voltage and capacitance-voltage characteristics were simulated at different temperatures and for the steady-state temperature distributions inside the transistors resulting from the self-heating effect during transistor operation. Two examples of numerical simulations are shown in figures 2 and 3.

Since the importance of self-heating increases for each new CMOS device generation, it is important to investigate self-heating effects in transistors that will be introduced in industry in the near future. For novel transistor architectures based on silicon-on-insulator technology, it was very important to account for a significantly lower thermal conductivity in thin silicon layers in comparison to bulk silicon when simulating self-heating. Also, thermal resistances between the transistors and the external area of a chip that is exposed to the ambient temperature have to be simulated taking into account the three-dimensional nature of the heat spreading. The simulations showed that there is a significant non-uniformity of the temperature in the active regions of SOI-based CMOS transistors during self-heating. An example of the simulated temperature distribution is shown in figure 4. Based on the results of numerical TCAD simulations, the extraction of thermally aware compact models was performed for SOI-based CMOS transistors with ITRS specifications for 2015. To allow the usage of the simulation results of this investigation in circuit design, a thermally aware compact model was extracted. The BSIM4SOI compact model was used for the simulation of the thermal effects in SOI transistors, because this model has special features to describe SOI transistors. The BSIM4SOI model allows circuit simulations of both stationary and dynamic thermal processes in CMOS integrated circuits. So we conclude that thermally aware compact models which extracted from the results of numerical simulations allow, in combination with a thermal circuit network, a simulation of thermal effects both inside a separate transistor and in larger integrated circuits.



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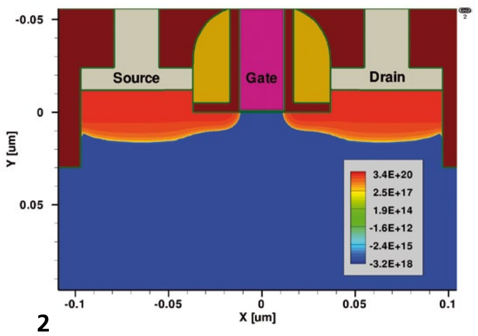
Content

1 *Energy dissipation density in the active areas of NMOS transistors (mW/µm²) for high-performance applications according to ITRS 2009.*



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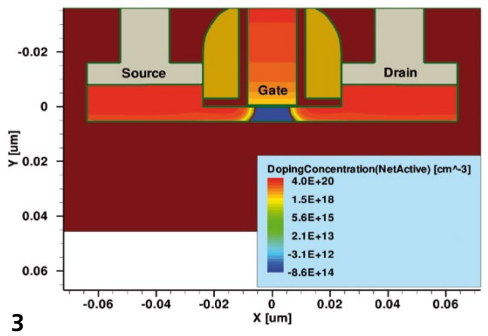

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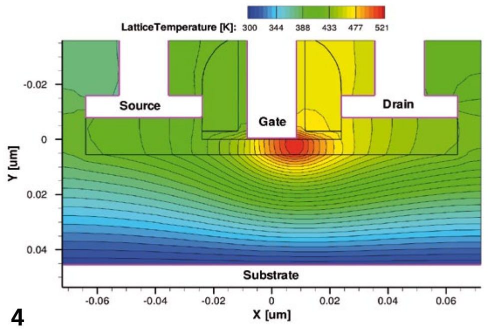

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2 *Simulated geometrical shape and doping distribution of a bulk silicon NMOSFET as specified by the ITRS for the year 2011.*

3 *Simulated geometrical shape and doping distribution of a fully depleted SOI NMOSFET as specified by the ITRS for the year 2015.*

4 *Temperature distribution due to self-heating in a fully depleted SOI NMOSFET-2015 in the on-state simulated using the improved model.*

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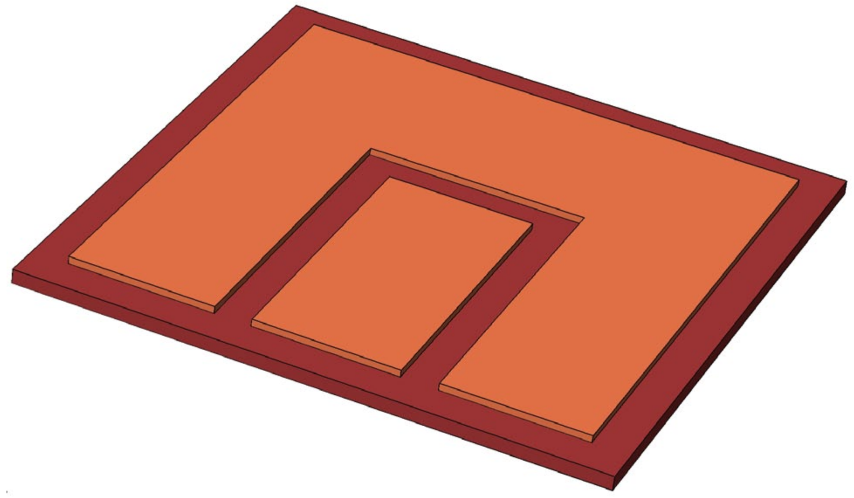

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Content

Simulation for Supporting Development of Substrates for Power Electronic Modules

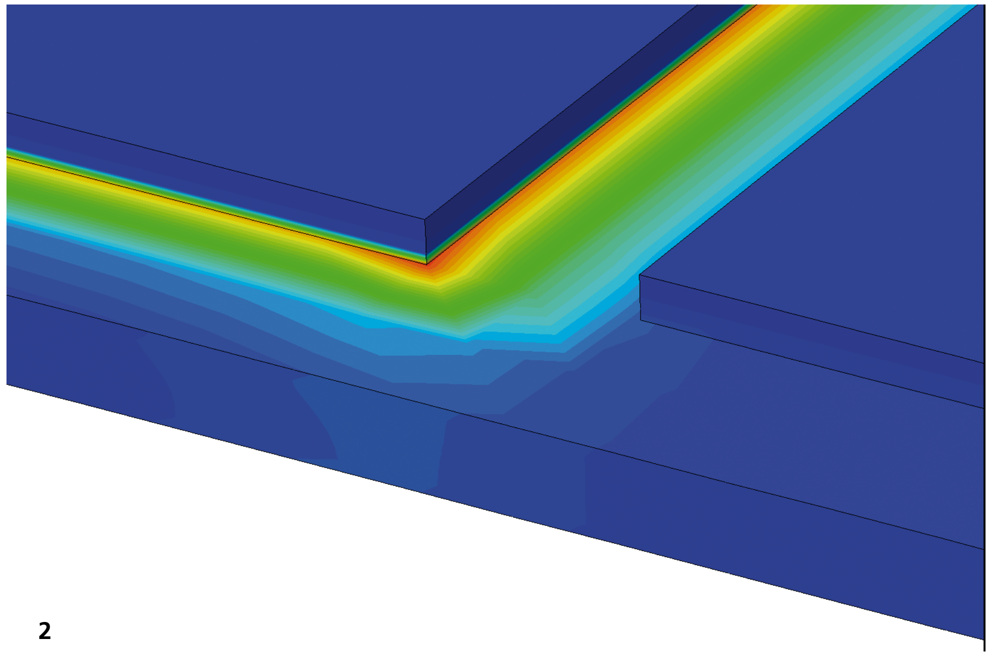
Advanced power electronic switches based on silicon carbide provide excellent energy saving perspectives for electrical power transmission systems. For such future power electronic modules, blocking voltages of several kilovolts (> 6.5 kV) and distances between electrodes of about one millimeter lead to high values of the electric field strength, possibly resulting in partial discharge which can lead to degradation. Simulation supports the investigation and optimization of different options in the design phase.

Partial discharge is an effect which occurs when the electric field strength locally exceeds a critical value in dielectric materials or gas enclosures. Charge transport takes place and may degrade the breakdown voltage. Different mechanisms are considered to be essential for explaining partial discharges. For all mechanisms, the maximum electric field strength is a determining factor. Therefore, the goal of the work presented here is to study the influence of modifications, such as that of the substrate geometry, on the resulting electric field strength.

Typically, the sequence of layers of a substrate is as follows (see also figure 1): At the bottom, a copper electrode serves as base plate on ground potential. The next layer is made of dielectric material, e.g. AlN or Al_2O_3. On top of the dielectric layer, the copper electrodes for mounting the power electronic devices are bonded. Large differences of the electric potential occur between the base plate and the top electrodes as well as between the different top electrodes. The peak values of the electric field strength are reached at the bottom edges of the top electrodes. The exact shape of the edges has a large impact on the resulting electric field strength. Geometrical effects which result from the processing steps used for etching the electrodes are thus very relevant. Rounding, tapering or incomplete etching resulting in footing needs to be considered for a realistic simulation. For our simulations, the substrate geometry has been created by using IISB´s in-house tool "ANETCH" (geometry emulator and physical etch simulator) combined with modules of the Synopsys TCAD framework. The electrical simulations have been carried out with Synopsys´ SDEVICE. An example for a simulation result is shown in figure 2. The red color corresponds to high values of the electric field strength.

The simulation example shown is based on an ideal geometry of the electrodes on the ceramic substrate. In reality, the shapes of the electrodes are not that ideal. The "ANETCH" tool allows us to physically model different etching processes and therefore to determine the realistic shape of the etched electrodes. In addition, other options modifying the geometry, such as variations of the layout or insertion of additional layers, can be studied as well. Also, small parts of the system could be investigated, for instance to study the effect of gas inclusions at material interfaces.

1 *Geometry of a substrate for power electronic modules. The ceramic layer is shown in dark red; the copper electrodes are colored in orange.*



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2 *Simulated distribution of the electric field for the substrate shown in figure 1 (close-up of area around one electrode edge). For the simulation, the potential of the outer electrode was set to 10 kV, whereas the inner electrode is grounded (see also figure 1 for displaying the different copper electrodes). The color contours representing the electric field strength range from blue (low) to red (high).*

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CRYSTAL GROWTH

Content

Focal Areas of Research and Development, Trends, and Potentials

The research focus of the Crystal Growth department is to clarify – in close collaboration with its industrial partners – how the material properties of bulk crystals as well as those of thin epitaxial or other functional layers correlate with their respective production conditions. The chosen strategy of IISB together with its subsidiary in Freiberg, the Fraunhofer Technology Centre for Semiconductor Materials (THM), is the optimization of crystal growth processes through a combination of thorough experimental process analysis and modeling. For that purpose, IISB and THM are provided with a well-suited infrastructure as well as with powerful and user-friendly simulation tools. These software codes which are tailored to the applications in the field of crystal growth are continuously maintained and enhanced in performance with regard to the needs of industrial partners.

In 2011, the Crystal Growth department of Fraunhofer IISB has consolidated its position as a worldwide acknowledged center of competence in the field of crystal growth.

In the field of crystallization of solar silicon, IISB together with its subsidiary in Freiberg, the Fraunhofer Technology Centre for Semiconductor Materials (THM), and its partners from industry and academia started to investigate how the directional solidification process for multicrystalline silicon ingots can be improved. Experiments were carried out in a lab-scale furnace at IISB and in a special R&D pilot plant scale furnace at THM with the goal to reduce detrimental dislocation clusters and grain boundaries. The reduction of these crystal defects is considered to close the currently existing efficiency gap between multicrystalline and monocrystalline materials. To solve this problem, the quantitative knowledge of e.g. the distribution of dislocations, the shape of the solid-liquid interface and the grain orientations and grain boundaries is mandatory. For that purpose, tailored metrology equipment was put into operation at THM.

In the field of crystallization of solar silicon, another topic is the analysis of the interaction of crucible materials and coating with silicon. A special furnace was developed and built which allows for example, the in-situ measurement of the contact angle between silicon and the crucible. As the standard silica crucible can be used only once in directional solidification of silicon, alternative crucible materials were tested. It could be shown that reusable crucibles exist. However, the reusability strongly depends on the crucible material. Furthermore, we started with the preparative work for an experiment to be carried out in space under microgravity conditions. The goal of this experiment is to analyze the interaction of foreign particles like SiC with the moving solid-liquid interface during the growth of silicon crystals.

In the field of wide band gap semiconductors, we started to support our industrial partner in the further development of the HVPE technique for growing GaN boules. The focus of the research activities is to improve the efficiency of the conversion of the precursors to GaN. Furthermore, valuable knowledge could be gained about the structural properties of free-standing GaN and of bulk crystals by using the high-resolution analytic tools available at IISB.

Within the framework of the BMBF cluster of excellence "Solarvalley Mitteldeutschland" we could make significant progress in the software and model development. Using the improved models, it was possible to reduce the process time of the cooling-down procedure during Czochralski growth of monocrystalline silicon by 30%. The coupling of global 2D and local 3D simulations by combining "CrysMAS" and "OpenFOAM" was applied to compute the heat and oxygen transport during Czochralski growth of 150kg heavy silicon crystals. The comparison with experimental data gave a very good agreement without any model adjustment.

A research award given to IISB strengthened the international reputation of the Crystal Growth department. Dipl. Ing. Ludwig Stockmeier received the Georg-Kurlbaum Award for his fundamental investigations of the directional solidification of quasi-monocrystalline silicon. Several invited talks during international conferences as well as the collaboration in different national and international expert panels in the field of crystal growth also underline the reputation of the Crystal Growth department. Further elements of the networking process were the events which were organized by IISB. Moreover, the Crystal Growth department works closely together with different research institutions and maintains national, but also international cooperations with industry.

1 *Dr. Jochen Friedrich, head of the department.*

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CRYSTAL GROWTH

1

Content

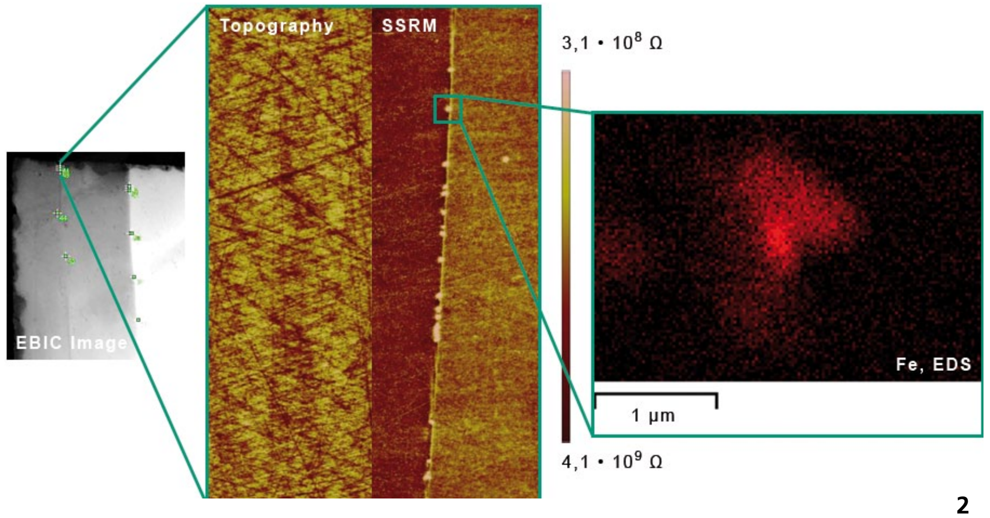
Investigations on the Iron Incorporation in Multi-crystalline Silicon Grown by Directional Solidification

The directional solidification of multicrystalline silicon ingots is a widely used technique for the production of photovoltaic silicon in PV industry. The pressure regarding production costs drives many attempts to improve the materialsquality by advanced thermal processing and a deeper understanding of the key defects influencing the performance of the final solar cell. The efficiency of solar cells of multicrystalline silicon (mc-Si) strongly depends on the electrical activity of crystal defects like dislocations, impurities and grain boundaries (GBs). Subsequently, the analysis of the electrical action of any defect like e.g. dislocations, impurities, grain boundaries, nitride or carbide inclusions or particles can enable a final understanding of the electrical response of the solar cell to these defects.

Transition metal contamination especially in form of iron is thought to be a major factor leading to the degradation of minority carrier lifetime in multicrystalline silicon. The iron contamination of the silicon ingots grown by directional solidification originates from different sources like the feedstock, the crucible and the crystallization furnace itself. However, it strongly depends on the state of existence of the iron in the silicon what the degradation effect would be. Though, we investigated in detail the influence of intentional contamination of multicrystalline solar silicon with iron by different means spanning the macroscopic to microscopic scale.

First, it was found that the development of the grain structure during the crystallization process does not change compared to uncontaminated material even at very high Fe contamination levels like some 1014/cm^3 which was disputed before (fig. 1). The carrier lifetime strongly drops with iron contamination which can be explained by the incorporation of the iron atoms on silicon lattice sites. In areas of the ingot where segregation of the metal takes place, the formation of iron precipitates is expected to form upon cooling of the crystal. High-resolution resistivity maps indicate that the resistivity of these types of material is lowered e.g. in the vicinity of grain boundaries. Electron beam-induced current measurements of such materials show discrete spots of no intensity where the carriers are locally recombined. The combination of very local analysis on the same location in an iron-contaminated sample gave direct evidence that precipitated iron along grain boundaries is responsible for carrier recombination and the lower resistivity of grain boundaries in iron-contaminated multicrystalline silicon which was not shown in this way before.

However, the correlative approach on the sub-µm scale is quite sophisticated, but extremely beneficial (fig. 2). The resistivity of the grain boundaries and precipitates was measured by scanning spreading resistance measurements (SSRM) at an AFM and the chemical nature of the precipitates was analyzed by high-resolution energy-dispersive x-ray analysis (EDS) applying a large angular drift chamber EDS detector.



2

1 *Grain structure of iron-contaminated multicrystalline silicon from directional solidification.*

2 *Direct evidence of Fe precipitates as carrier recombination centers and cause for low-resistivity grain boundaries in multicrystalline solar silicon by direct correlation of EBIC, EDS and SSRM on the sub-µm scale.*

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Content

Low-cost Gallium Nitride Crystals

Gallium nitride (GaN) has myriad uses including low-energy light sources (white and blue LEDs), mobile communications (efficient amplification and fast data transmission), and power converters in low-loss, highly efficient power devices (in computer power supplies, in photovoltaics or in the electric vehicles of the future).

GaN is currently used in white and blue LEDs in the form of a thin epitaxial layer that is deposited onto a substrate of sapphire or silicon carbide. Large physical and chemical differences between the substrate and the GaN layer above it lead, however, to a great number of structural defects (dislocations) in the deposited layer. The LEDs continue to work, however, although the number of defects in the crystal can be higher than 1 billion per cm².

High-performance devices like blue lasers found in blue-ray players or the high-efficiency devices needed in power electronics or in mobile communications need better material to show good device performance. This is because their output and reliability can be severely impaired, if there are more than a thousand defects per cm² in the active layer. In such cases, it is necessary to deposit the active layers on single-crystalline GaN substrates of the same type.

Substrates of this kind are very expensive today. A GaN substrate with a diameter of 50 mm is worth more than ten times its weight in gold. The high manufacturing costs are an obstacle to this semiconductor material becoming commercially viable. Another complicating factor is that large GaN single crystals are still not available in sufficient quantities, as their production is very difficult. Due to its high melting point (over 2500 °C) and the high vapor pressure (over 100,000 bar) at the theoretical melting point, GaN cannot be produced using the classic melt growth method.

Scientists and a handful of commercial manufacturers use the HVPE (hydride vapor-phase epitaxy) method instead to produce GaN single crystals. This technique applies chemical gas-phase reactions to deposit GaN and is a special kind of CVD process. First, gaseous hydrogen chloride is reacting with liquid gallium at about 880°C and is forming gallium chloride. This gaseous gallium chloride is convecting inside the reaction chamber to a GaN seed crystal which is heated to about 1100°C. Then, ammonia is introduced into the reaction chamber. The ammonia converts the GaCl into GaN while releasing HCl. The GaN is epitaxially deposited on the seed crystal. Currently, under optimum conditions, HVPE processes can realize GaN crystals with a diameter of 50 mm and a thickness of several millimeters.

Unfortunately, like all gas-phase epitaxial processes, the HVPE process has a low yield. Currently, only a few percent of the gaseous precursors – gallium chloride and ammonia – react to form GaN at the right place. This is one of the main reasons for the presently high manufacturing costs.

Together with our industrial partner, we are further developing the HVPE process to ensure that the materials used can be converted to GaN more efficiently. This is done by improving the design of the reaction chamber, numerical modeling of the gas-phase reactions and applying extensive in-situ characterization of the process.

This could reduce manufacturing costs and drive forward the commercial viability of GaN. The project with a duration of three years is funded by the Saxon State Ministry for Higher Education, Research and the Arts using money from the European Fund for Regional Development and from the Free State of Saxony.

1 *Test system at Fraunhofer IISB for accompanying studies on increasing material efficiency in HVPE GaN crystal growth.*

2 *GaN crystals grown spontaneously from a gaseous state; the grid is 1 mm.*

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Content

Ultra-fast, Full Wafer-scale Mapping of Grain Structure, Orientation, and Boundaries of Multi-crystalline Silicon Wafers

Wafer-based silicon solar cells are dominating the absorber market (~90%) for photovoltaic applications today and in the next decade. For the manufacturing process, cost-effective silicon crystals with customized properties are used which are cut into thin silicon wafers for solar cell production.

Directional solidification techniques are widely used for the production of multi-crystalline silicon ingots. A silicon melt with temperatures around 1450°C is contained in a square-shaped crucible and solidified from the bottom to the top.

The revealed grain structure of crystalline silicon ingots can vary depending on the used growth condition and also on the ingot position. Advanced crystal growth processes are under development to improve the material quality by influencing the grain growth in order to reduce the defect densities and to increase the grain size.

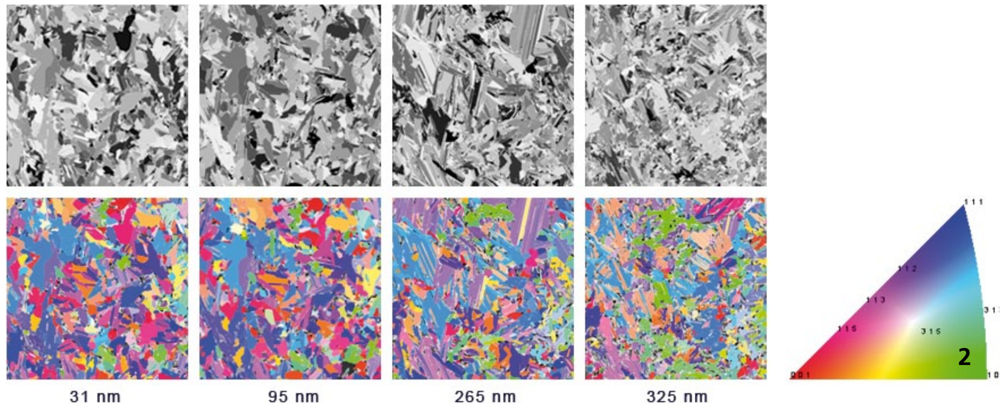
But: How can we characterize the grain structure of the different wafer materials for an effective process development and wafer material classification?

Existing characterization tools like Electron Backscatter Diffraction or simple reflectivity measurements cannot provide the information needed about grain size and distribution, grain orientation, and grain boundary configuration on the full wafer scale in short time scales.

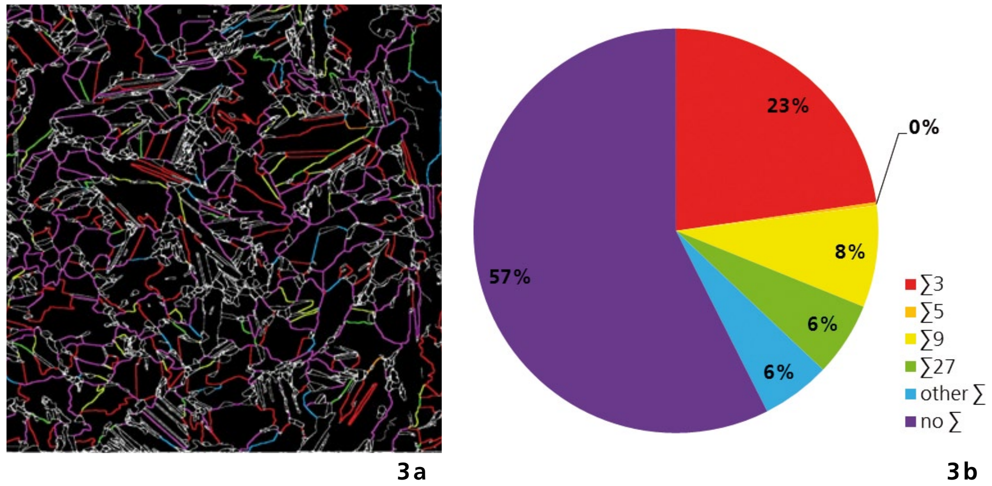
Therefore, Fraunhofer IISB and the subsidiary THM in Freiberg developed in collaboration with Intego GmbH and GE Sensing & Inspection Technologies GmbH a new characterization tool combining a Grain Detector and an Orientation Scanner. Reflectivity measurements under different illumination scenarios lead to an effective detection of the grains and grain boundaries on standard as-cut wafer material with a size of 156 mm² within 10 s. The Orientation-Scanner uses the Laue x-ray method to measure the crystal orientation matrix for every single grain on the wafer using the grain data generated before from the Grain Detector. Further post processing gives the grain orientation perpendicular to the wafer surface and the boundary types in between neighboring grains. The minimum measurable grain size is in the range of 1 mm². Measurement times per standard multi-crystalline wafer with typically ~500 grains are in the range of 3 - 4 hours. Single wafer investigations are even possible like batch analysis.

First results on multi-crystalline silicon wafers from different ingot heights show the potential of this system as an effective characterization tool for the investigation of the crystal texture of directionally solidified crystalline silicon. Therefore, the system can help to further improve industrial crystallization processes and can give values for wafer classification processes. The development activities at Fraunhofer IISB and THM were honored with the Fraunhofer IISB R&D Team Award 2011.

1 *Orientation scanner. Image: GE Sensing & Inspection Technologies GmbH.*



2 *Highly contrasted grain structure and RGB color-coded measured axial grain orientations perpendicular to the wafer surface for different 156 mm²-sized wafers over the ingot height.*



3 *a) Mapping of the different grain boundary types on a 156 mm²-sized multi-crystalline silicon wafer,*
b) statistics on the amount of grain boundary types.

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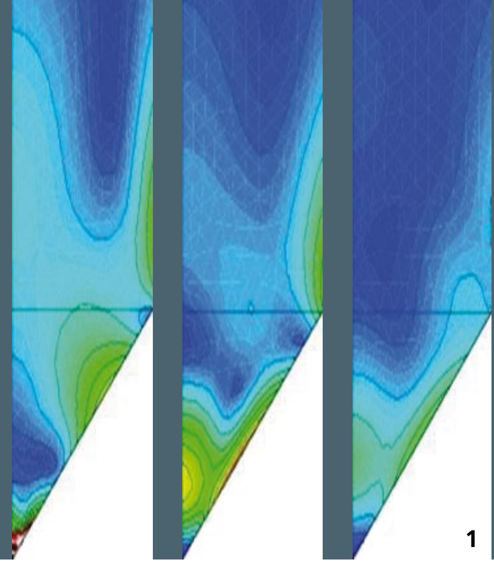
Optimization of the Cooling-down Phase During Czochralski Crystal Growth of Silicon Crystals

The Czochralski growth of silicon crystals is widely used for the production of wafer material for electronics and photovoltaics applications. The competition among material producers emphasizes the need for a reduction of process costs and an increase of material quality.

One key activity of the crystal growth numeric group is to support these developments by numerical simulations. Our numerical models describe heat and mass transfer in order to optimize the furnace design and the crystal growth process. Besides detailed studies of e.g. the highly turbulent melt flow, dopant concentrations and radiative heat exchange, process optimization also includes the analysis of stress and the resulting generation of dislocations in the crystal. Especially, the formation of dislocations explicitly depends on the thermal history of the growing crystal. Therefore, also the cooling-down phase after finishing the Czochralski crystal growth is of importance for the final material quality in terms of defects and dislocations. In recent years, a trend towards thinner wafers is observed. This involves additional requirements on the residual material stress in order to avoid breakage during wafer-handling.

In the “CzSil” project, which is part of the BMBF excellence cluster “Solarvalley”, we were involved in the investigation of various options to increase the quality of silicon wafers for photovoltaic applications while reducing production costs at the same time. Regarding the optimization of the cooling-down phase, we could show that a reduction of the cool-down time by 30% is possible without introducing additional dislocations.

As an example, in the graphs on the left, our optimized process is compared to an standard industrial process. In the optimized process, we find that after a critical initial stage the process time is mainly limited by the thermal inertia of the furnace. For the generation of dislocations , the critical resolved shear stress (CRSS) is used as criterion. The CRSS is a temperature-dependent empirical correlation which describes the critical stress where plastic deformations occur and dislocations are generated. Thus, the thermal stress induced in the crystal, described in terms of the von-Mises stress, should not exceed the CRSS. Our simulations show that the ratio von-Mises/CRSS in the crystal tip region is about a factor of two larger than in the cylindrical region which is used for wafering. This is illustrated in a more detailed way in the colored figures on the left, where the distribution of the von-Mises/CRSS ratio in the crystal is shown for times of 60s, 300s and 2500s after removing the crystal tip from the melt surface.



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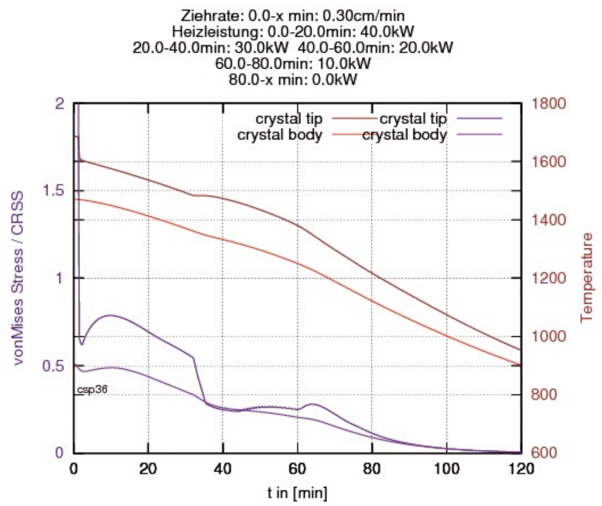
Content

To obtain these results, a new feature to describe moving geometric elements within time-dependent simulations was added to our software package “CrysMAS”. The prerequisite for this feature is the update of the numerical mesh and the view factors for radiative heat exchange in every time step. Especially the continuous update of the view factors is numerically expensive and requires an HPC facility.



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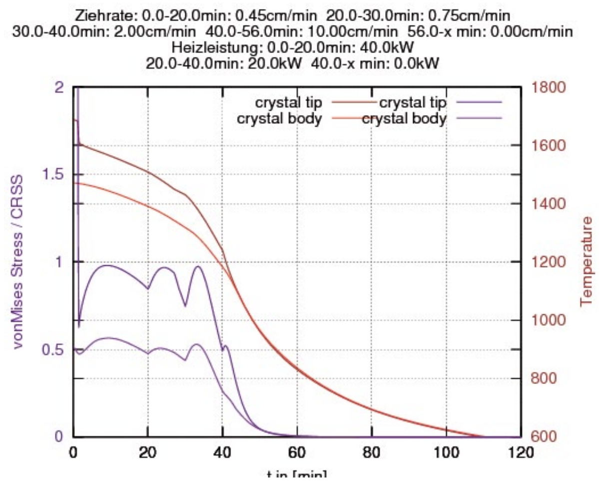

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1 *Distribution of the von-Mises/CRSS ratio in the crystal for 60 s, 300 s and 2500 s after removing the crystal tip from the melt surface.*

2 *Mean temperature and von-Mises stress/CRSS ratio in the crystal tip and the crystal body for*
a) an standard industrial process and
b) an optimized process.

SEMICONDUCTOR MANUFACTURING EQUIPMENT AND METHODS

Focal Areas of Research and Development, Trends, and Potentials

The core competence of the department "Semiconductor manufacturing equipment and methods" is the multidisciplinary research and development for manufacturers of equipment, materials, and semiconductor devices. The decisive factor for this is the expertise in process development, metrology, analytics, software, simulation, and device integration combined to develop tailor-made solutions together with customers.

For this approach, a wide-ranging expertise is essential which manifests itself in the competence area regarding equipment, advanced process control, manufacturing control, productivity, contamination, and materials. Experts from the fields of electrical engineering, materials science, physics, chemistry, and computer science work together on the issues that will sustainably influence efficiency in the construction of manufacturing equipment, the production of materials for manufacturing, and IC manufacturing itself.

The scope of developments ranges from lead research for novel processes and measurement methods to the application of new research results in cooperation with corporate partners and to the assessment and optimization of equipment in an industry-compliant environment. Essential for a conclusive and comprehensible assessment is the successful accreditation of IISB's testing laboratory according to DIN EN ISO 17025 (described in detail below) in 2009. For this, the participation in the European distributed laboratory "ANNA", a project which will be completed in 2011, was essential.

Preliminary research in the reporting period includes, for example, the development for UV-based measurement of thinnest layers under vacuum conditions or the development of a polishing head equipped with sensors for characterizing CMP processes. During the reporting period, the successor of the successful "SEA-NET" project was launched: the EU project "SEAL" again aims at developing and evaluating innovative process and metrology equipment in a European network of 35 equipment suppliers, device manufacturers and research institutions to make them ready for series production.

The ENIAC project "IMPROVE", which aims at doing research in the field of cutting-edge methods for increasing the efficiency of domestic and European semiconductor manufacturing, is almost finished. Research approaches and first results are presented in a separate report. Reaching far into the future, the ENIAC project "EEMI 450" works on the specification and preliminary development of equipment and materials for the upcoming production on 450 mm silicon wafers (see separate report).

Successfully completed collaborations like "NANOCMOS", "PULLNANO" or "SEA-NET", as well as ongoing projects such as "ANNA", "SEAL", "IMPROVE" and "EEMI 450" make highest demands – especially in the European context – on knowledge and communication skills of the researchers involved: automated process control, integrated and virtual metrology, yield optimization, predictive maintenance, throughput optimization, device integration, 450 mm processes and devices as well as simulation of manufacturing equipment and components are just some of the challenges that can only be met successfully in a multidisciplinary approach. Research projects of this kind as well as bilateral development projects with industrial partners confirm the broad approach of the department which is well-positioned for the future due to its variety of topics.

The described research activities are complemented by the involvement in local and international committees and panels: staff members of the department are active in several committees and sections of the "VDI/VDE-Fachgesellschaft GMM" and take leadership roles in the development of SEMI standards and the ITRS, the International Technology Roadmap for Semiconductors.

1 *Prof. Lothar Pfitzner, head of the department.*

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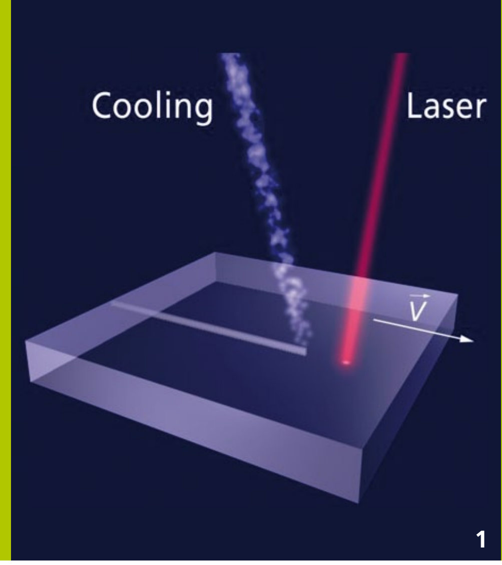

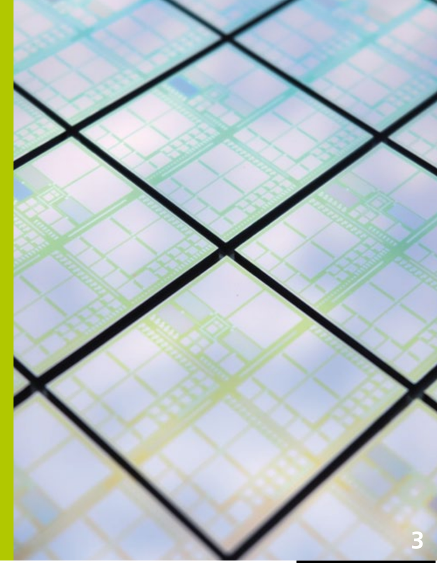

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Thermal Laser Separation – from R&D to Applications

After developing the basic technology within the integrated project "SEA-NET" (finalized in 2009, see the respective annual report for details), the innovative dicing technology "Thermal Laser Separation" (TLS) has been further optimized in close collaboration with the equipment supplier "JENOPTIK Automatisierungstechnik GmbH". Results of research and development were successfully transferred to customer-specific applications.

TLS is a laser-based dicing technology for separating brittle materials like silicon (Si) or other semiconductor wafers. The chips on a wafer are separated not by sawing or ablation, but by a defined cleaving of the wafer. Laser-based heating and immediate subsequent cooling locally induce mechanical stress inside the wafer. This mechanical stress is capable of guiding a crack through the wafer following the path of the heating/cooling spot. TLS is an ablation-free and hence kerf-free separation process which generates perfectly smooth edges. Such a high-edge quality results in high bending strength of the separated chips, which is important e.g. for RFID products and security smart chip cards. Further products that need perfect edges are semiconductor laser diodes. Laser diodes emit radiation from one of the produced side walls which have to be perfectly smooth and clean. Otherwise, the laser device would emit laser light of poor quality. In addition, a zero kerf width allows a closer packing of a larger number of chips per wafer.

After the successful completion of the TLS equipment assessment in 2009, Jenoptik and the Fraunhofer IISB continued their close cooperation in further process optimization and application development to make the potential of this innovative dicing technology widely available. Process optimization is being done with the latest version of the TLS dicer, which serves as technology platform at the IISB cleanroom facility. Major R&D topics focus on further improving the crack guiding by the heating/cooling combination and special subjects like circular cuts for resizing crystalline Si wafers.

Results of the research are continuously being transferred to customer-specific applications, using especially the perfect TLS edge and the kerf-free separation. Examples for specific applications are as follows:

TLS for dicing through the "heart" of Si-based diodes without damaging the product

We could demonstrate that TLS is capable of dicing Si-based diodes cutting directly through the pn junction, which is the "heart" of the diode, without deteriorating the electric behavior of the diodes. That allows for omitting currently necessary protection processes and hence improving the cycle time.

High-speed dicing of SiC wafers with feed rates of up to 200 mm/s

SiC is almost as hard as diamond. That is why the current state-of-the-art mechanical wafer dicing which uses diamond blades results in both a poor throughput and in a poor edge quality as well. Approximately one dicing blade is needed for dicing a single 100 mm SiC wafer with a feed rate of 1-2mm/s.

Using TLS, 100 mm SiC wafers with a total thickness of 450 µm could be separated for the first time with feed rates up to 200 mm/s. That is an improvement of a factor of almost 200. Besides the vastly improved dicing speed, the TLS edges are free of chipping hence leaving behind an absolutely smooth edge.

Breaking single-crystalline silicon substrates in a circular shape with TLS

TLS allows for free form cutting. The TLS crack is not bound to the crystallographic planes. In fact, it is possible to break single-crystalline Si substrates in a circular shape. That is important for resizing Si wafers to smaller diameters. During the transition to the next wafer diameter of 450mm, wafers of new sizes have to be easily adapted to fit e.g. currently available metrology and process equipment. For the first time, circular cuts with diameters of up to 300 mm were produced out of 450 mm (thickness: 925 µm) single-crystalline Si wafers with TLS.

Further equipment optimization and process development is going on in close collaboration between "JENOPTIK Automatisierungstechnik GmbH", Fraunhofer IISB and the respective industrial partners to make the potential of the TLS technology widely available.

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1 *Principle of Thermal Laser Separation. Image: JENOPTIK Automatisierungstechnik GmbH.*

2 *TLS process result for resizing a 300 mm single-crystalline Si bare wafer to a diameter of 200 mm.*

3 *TLS process result for separating integrated circuits.*

SEMICONDUCTOR MANUFACTURING EQUIPMENT AND METHODS

1 *Participants of the „SEAL" kick-off meeting at Fraunhofer IISB.*

Content

SEAL – Succesful Start of a Powerful Joint European Project to Foster the European Semiconductor Equipment Industry

The joint European project "SEAL" (Semiconductor Equipment Assessment Leveraging Innovation) dedicated to foster the European semiconductor equipment industry on a global market has been started successfully.

The objective of this project is to speed up the market maturity of innovative and production-ready equipment and to foster cost-effective equipment development in strong cooperation with equipment users, materials manufacturers and IC manufacturers. SEAL supports networking and cooperation between equipment producers and users as well as creates synergies between all partners to be successful on a global market. In total, 38 project partners including major European semiconductor equipment manufacturers, materials manufacturers, major IC manufacturers, innovative start-ups and well-known research institutes, started the joint EC-funded project "SEAL" on semiconductor equipment development and assessment. The coordinator of the project is the Fraunhofer Institute for Integrated Systems and Device Technology (IISB) in Erlangen. The IISB has broad experience in the coordination of such big projects and has already successfully coordinated the predecessor project "SEA-NET".

Semiconductor equipment is required for the production of all kinds of semiconductor devices like microprocessors, memories, MEMS, or sensors. Nearly in every electrical device, machine, and facility, these semiconductor devices or chips are inevitable for controlling, storage, display, or measuring. Examples are mobile phones, PCs or cars. Innovative semiconductor manufacturing equipment is the key for the production of such chips or devices with steadily increasing functionality, energy efficiency, and performance. Today, the investment necessary for a leading-edge semiconductor manufacturing plant is about 3 billion euros. About three quarters of this investment is covered by equipment. To foster the development of innovative equipment, to reduce the time to make this equipment ready for production, and finally to foster the European semiconductor equipment industry on a global market are the ambitious goals of SEAL.

Experience has shown that equipment-oriented activities have a lot in common in the area of process characterization, process optimization and readiness for advanced control methods. All equipment types face similar challenges and opportunities in the area of equipment characterization, equipment simulation, and automation – both with regard to hardware (such as robotics and wafer handling) and software. Therefore, a cross-cut R&D sub-project was included in "SEAL" providing the glue between all sub-projects. The main objective of this sub-project is to identify common problems and challenges amongst the "SEAL" sub-projects, and to work on overall and sustainable solutions. Several common challenges have been identified during the proposal set-up of "SEAL" and new ones were added after starting. The work covers, among others, predictive maintenance, plasma simulation, discrete event simulation, cost-of-ownership calculations and equipment assessment metrics.

Some facts on SEAL:

- 18 different production and metrology equipment systems of the latest technology are developed and assessed in a joint new approach.
- „SEAL" combines advanced R&D topics with equipment assessment involving a wide community of equipment suppliers, material manufacturers, semiconductor manufacturers and research institutes.
- „SEAL" integrates renowned R&D institutes to provide dedicated development support and innovative approaches covering equipment and process characterization, virtual metrology, application of advanced process control, and discrete event simulation.
- „SEAL" will strengthen the European equipment manufacturing industry in an efficient and sustainable way.
- „SEAL" especially strengthens the small and medium-sized companies (SMEs) by establishing a valuable network with European materials manufacturers, major semiconductor manufacturers and research institutes. Over one third of the equipment suppliers are SMEs.
- „SEAL" will enhance the prospects for the successful introduction of proven leading-edge European equipment to the global market.

"SEAL" is a 3-years project with a total budget of more than 14 million euros with considerable funding of 9 million euros from the European Commission under the contract number 257379. All partners are grateful to the European Commission for funding this innovative project aiming at fostering the European equipment and materials industry.

Additional information can be found at www.seal-project.eu.

SEAL Semiconductor Equipment Assessment Leveraging Innovat

SEVENTH FRAMEWORK PROGRAMME

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SEMICONDUCTOR MANUFACTURING EQUIPMENT AND METHODS

Predictive Sampling

Semiconductor manufacturing is a highly complex value-added process, which is facing an extreme cost pressure due to fast-changing markets combined with very high capital investments. Currently, a manufacturing cost reduction of 15 % per year has to be achieved by increased equipment and fab productivity in order to compete on the global market.

One contribution for achieving a cost reduction in semiconductor manufacturing is to reduce the effort for defect density control operations. Nevertheless, the reduction of control operations has to be done without increasing the risk of not detecting any process abnormality as early as possible. The challenge is to develop effective sampling strategies, which need minimized control operations and are capable to rapidly find defective products or tools before out-of-specification lots are processed.

Development approach and results

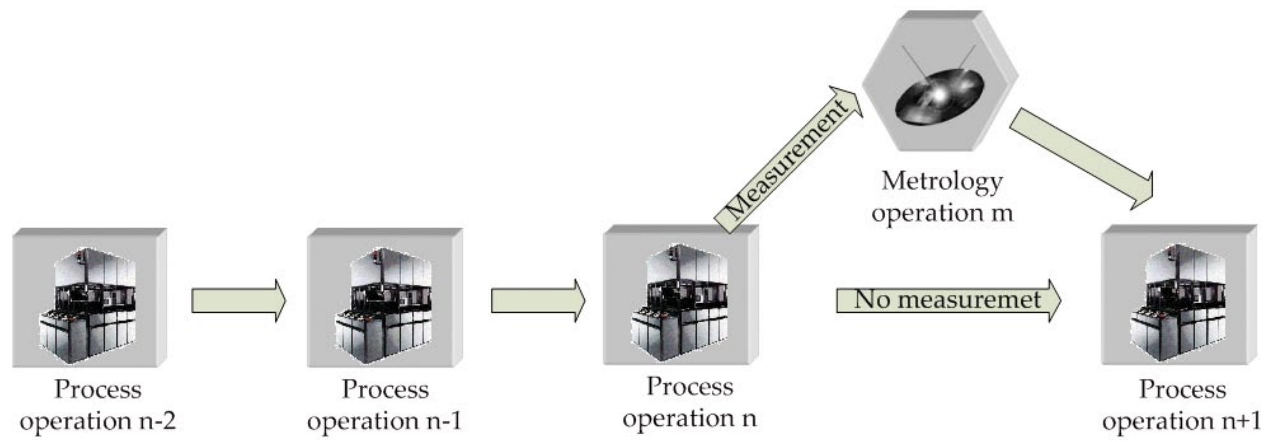
On process sequence level, investigations regarding sampling strategies were performed and an innovative predictive sampling strategy (PdS) was developed. This strategy dynamically adapts the sampling to the current fab situation. The predictive sampling strategy is based on a metrology chain concept, which means that several subsequent process operations (up to 20) will be validated by a single metrology operation afterwards. This concept is shown in principle in figure 1.

The sampling decision is based on this prediction, if it is possible to keep the risk expressed by the wafer at risk (W@R) below a given warning limit even without performing a defect density control of the current lot until the next lot could be measured. The decision is made after the last process operation n in the given example (figure 1).

The predictive sampling strategy offers a great potential to reduce manufacturing costs by reducing the amount of required defect density control operations. Furthermore, the risk of uncontrolled manufacturing equipment could also be decreased. The developed predictive sampling strategy was evaluated using real historical fab data from different Infineon manufacturing sites. For the investigated applications, the number of required defect density measurements could be reduced by up to 65 % compared to the sampling strategies, which are currently used at the evaluated semiconductor manufacturing sites. At the same time, the risk of uncontrolled process operations could be reduced by up to 45 %. Exemplary results of the predictive sampling strategy are shown for tool control in figure 2 and for technology control in figure 3.

Summary

The application of the developed predictive sampling strategy provides an optimized tool or technology control (less W@R excursions) and a reduced effort for defect density control operations.



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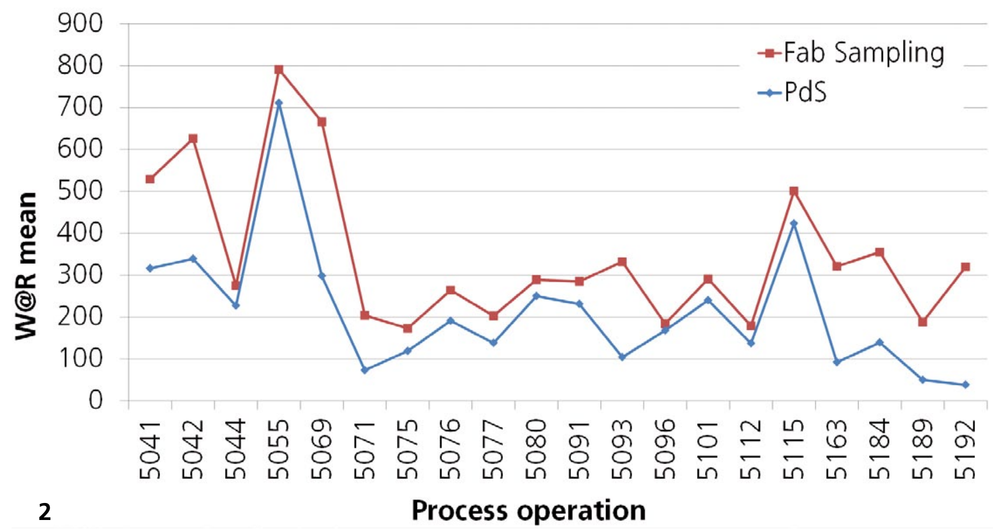
1 *Principle of an analyzed metrology chain.*



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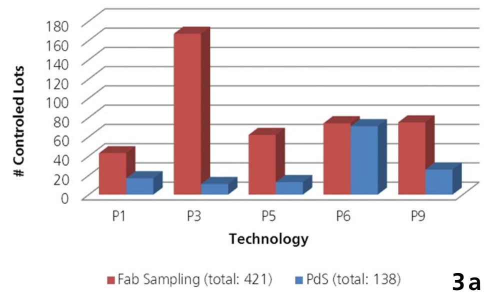
2 *Mean W@R for a whole metrology chain for PdS (predictive sampling) and for historical fab sampling.*



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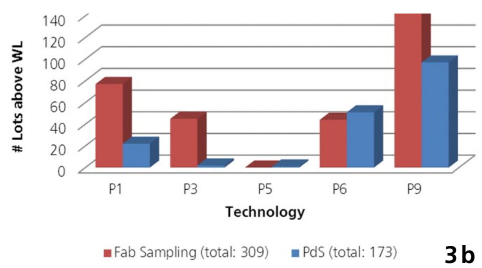

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3 *a) Number of performed control operations using fab sampling and PdS strategy, b) Number of lots with risk excursion using fab sampling and PdS strategy.*

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Content

TECHNOLOGY

Content

Focal Areas of Research and Development, Trends, and Potentials

Above all, technology stands for research and development in the field of electronic devices on all dimensional scales, but also for facility services for customers. From nano technology to printable macroelectronics, the technology department is your contact for the realization and characterization of single process steps and devices up to prototypes. Based on comprehensive cleanroom facilities, the silicon as well as the silicon-carbide processing forms the backbone of the technology. Examples for current activities are highly resolved electrical characterization of novel dielectric layers, the development of tailored ion implantation processes, advanced integrated power devices, low-temperature deposition of inorganic materials by printing techniques or the preparation of nanostructures with focused ion beam technology. The heterogeneous integration of various technologies gains more and more importance.

For this purpose, IISB and the Chair of Electron Devices of the University of Erlangen-Nuremberg operate joint cleanroom facilities of 600 m² (class 10) provided with CMOS-compatible equipment. This allows the implementation of the most important process steps on silicon wafers with diameters of up to 200 mm. An industrial CMOS process transferred to IISB and adapted to research and development purposes is used as reference and basis for the development of advanced process technologies.

For the development of novel process steps in the field of gate stack engineering, IISB operates advanced sputter and chemical vapor deposition tools on the basis of ALD and MOCVD for the deposition of high-k and metallic layers. Adaptation of the process to the particular chemistry of the precursor, deposition of a multiplicity of precursors, and the characterization of the deposited layers are main tasks of the department. Special activities are focused on ion implantation technologies. At IISB, implantation tools with acceleration voltages of some eV up to several MeV are available. Special implantations for CMOS as well as for power semiconductors have been established (e.g. commercial tools have been modified to be able to implant several wafer diameters and manifold elements at elevated temperatures).

Further activities focus on the fields of power semiconductors and silicon-carbide electronics. IISB has increased its commitment in these fields by implementing new equipment and processes to meet special requirements necessary for Si and SiC power devices. Above all, it is etching and refilling of deep trenches and high-temperature processing of SiC. A Smart Power IGBT technology with integrated trench isolation has been implemented successfully. This allows the department to strengthen its competence in manufacturing smart-power or high-voltage devices. In the meantime, the IISB can perform nearly all manufacturing steps on SiC substrates. Devices under development are chemical gas sensors on a MOSFET basis with attached logic gates for high-temperature applications and power devices like vertical or lateral DMOS.

Physical characterization of process steps and device structures is of utmost importance for the manufacturing of semiconductor devices. Important steps in this respect are the determination of composition, topography, doping profile, and further physical and chemical parameters as well as SEM & TEM investigations, energy-dispersive X-ray analysis, and AFM surface characterization of layers. The specific competence of the department is the combination of several methods for failure analysis during the processing of semiconductor devices or tracing of failure causes. The spectrum for electrical characterization has been further increased (e.g. lifetime measurements).

Another focal area of the department's work is the processing of structures in the range of a few nanometers as well as the repair and analysis of prototypes of electronic devices with focused ion beam (FIB) techniques and electron beams. In addition to that, nanoprobes for atomic force microscopy are developed by using FIB to determine physical and chemical parameters like doping profiles or layer properties with a much higher resolution. Based on these experiences, models have been developed describing the collateral modifications of the substrates outside the purposely irradiated areas.

The focus of the activities in the field of printable electronics is the investigation and development of manufacturing methods for solution processing of inorganic thin films for electronics. A special focus is set on the interaction of processing and the resulting electrical properties of the application. Based on inks with semiconducting, conducting, and insulating nanoparticles or the respective molecular precursors, thin-film transistors (TFTs) comprising printed features are realized and the properties of functional thin films made by means of liquid processing are analyzed in detail.

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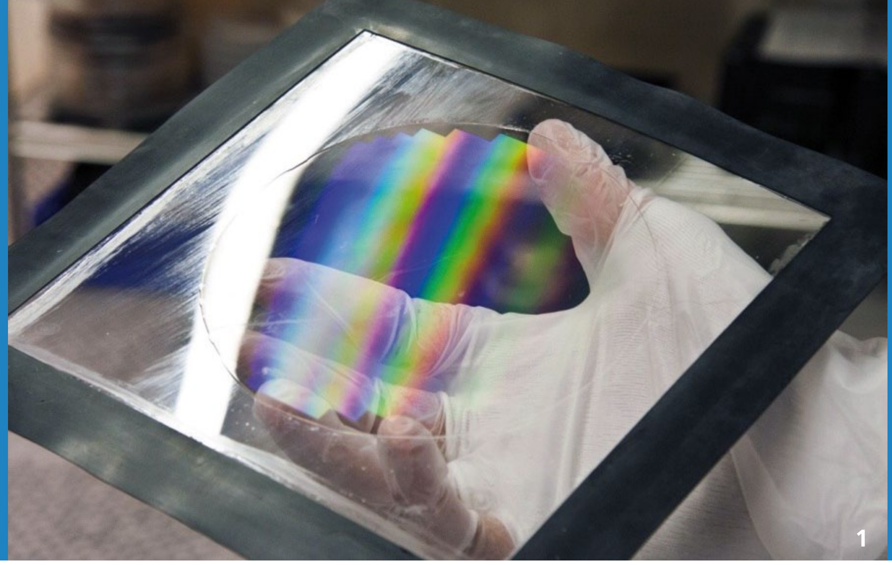

Content

Substrate Conformal Imprint Lithography of Functional Materials

Substrate conformal imprint lithography (SCIL) is a new and highly innovative nanoimprint technology on full wafer scale for the transfer of nanostructures into a liquid resist applied on the substrate. This sub-micrometer patterning method uses flexible wafer-scale PDMS stamps for the structure transfer. These stamps were sequentially exposed to the coated substrate and enable the nanostructuring of a full wafer in one single step. Originally, SCIL technology was developed for the transfer of structures into sol-gel materials which are hardened via out-diffusion of the solvents into the PDMS stamp material. Recently, UV-curable materials have been introduced as resists for enabling UV-enhanced SCIL (UV-SCIL).

For the further development of this powerful technology and to make it ready for the market, Fraunhofer IISB together with the company SUSS MicroTec initiated the project "Substrate Conformal Imprint Lithography of Functional Materials" (SILFUMA) which was funded by the "Bavarian Research Foundation". As associated partners, the companies "DELO Industrial Adhesives" and "micro resist technologys" substantially supported the project. Three main objectives have been worked out: the simplification of the PDMS stamp manufacturing, the evaluation of purely organic resists for UV-SCIL with short curing times and the development of a functional resist material for the direct imprinting of functional elements.

The first part of the project was the simplification of the stamp manufacturing. Molding of the fragile PDMS stamps from master structures is a process with several complex steps which needs experience. Even then, however, many stamp rejections arise, because most of the manufacturing steps can cause defects on the stamp. During the work, the stamp manufacturing process was simplified and the manufacturing tools were redesigned in order to make them more applicable. The reworked tools and the developed process allow to produce defect-free stamps with a lifetime of more than 500 imprints for the first time (see fig. 1).

The second objective was the evaluation of purely organic resists for UV-SCIL. Up to now, commonly used resists for SCIL or UV-SCIL contain inorganic chemistry. This fact limits their suitability for dry etching processes. Furthermore, all common resists for SCIL or UV-SCIL need long curing times (3min. – 15min.). However, purely organic materials are well-suited results of the work, two UV-SCIL processes with purely organic UV polymers, one with mr-UVCur06 from "micro resist technologys" and one with DELO-KATIOBOND OM VE 110707 from "DELO Industrial Adhesives", could be developed within this project. With DELO-KATIOBOND OM VE 110707, it was possible to reduce the curing time down to 17s and thus to reduce the overall process time essentially. Differential scanning calorimetry of the cross linking reaction of DELO-KATIOBOND OM VE 110707 showed that using an electrically heated chuck allows even a further decrease of the curing time down to 5s. This short curing time was realized within the project.

The third main objective of the work was the development of a functional resist material and its associated UV-SCIL process. A common structure transfer process of a functional layer needs a structured resist layer on top as mask for the etch process which transfers the desired structure onto the substrate. If the resist acts as functional material, the etch process step can be saved. Functional configurations are produced directly with such a resist by UV-SCIL. But the functional material needs to be designed in a way that it has the properties adapted for the functional element like a certain electrical conductivity, a certain permittivity, or a certain refractive index. One way to achieve it is to add nanoparticles to the resist. Therefore, two different kinds of nanoparticles (silver for conducting and silicon dioxide for insulating layers) were mixed with polymer matrix materials and after that an UV-SCIL process with these materials was developed. The experiments showed that the direct imprinting of functional elements is now possible and that these novel resists enable new applications for UV-SCIL.

UV-SCIL technology has been improved significantly and its application has been extended to functional materials which will be used in future technologies.

1 *Flexible 150 mm UV-SCIL PDMS stamp with wafer-scale pillar patterns (diameter of 2 µm).*

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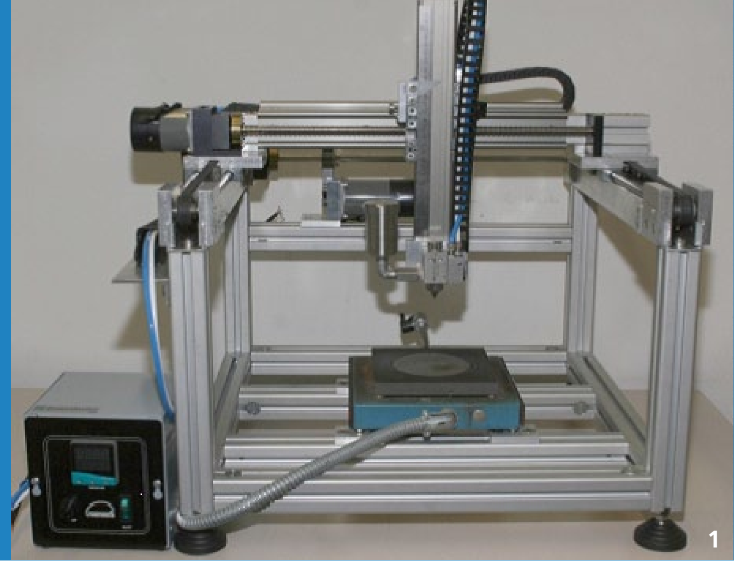


Content

Ambient Air Deposition of Functional Thin Films

Thin films for microelectronic and nanoelectronic applications are usually deposited with high technological effort under vacuum and mostly at high temperatures. A low-cost spray technique developed at IISB enables the deposition of semiconductors for large-area electronics under ambient air conditions. The technique can be used far beyond electronic applications by proper choice of the precursor chemistry.

Metal oxides like zinc or tin oxide are increasingly used for the realization of the basic features of electron devices and circuits in low-cost and large-area application. The properties of semiconducting, conducting and insulating thin films can be tailored by mixing or doping of various metal oxide materials. In addition, most metal oxides are transparent due to their electronic structure and thus are highly suitable for their application in optoelectronics and electronics. To date, metal oxides made by means of conventional vacuum techniques are widely used as transparent areal electrodes in displays, thin-film photovoltaics, and OLED lighting devices.

Besides physical or chemical vapor deposition, many techniques are available for the chemical synthesis of metal oxide nanomaterials and thin films. High-volume production of zinc oxide or titania nanoparticles is well established for a long time already and is the basis for emulsion paints or cosmetics. Current research at IISB focuses on the possibility of depositing the precursors directly onto the sample and performing their transformation into metal-oxide thin films directly on the substrate. Among other techniques, this is mainly achieved by means of an in-house developed spray-coating system (fig. 1). A high level of automation allows for precise control and reproducibility of the deposition processes.

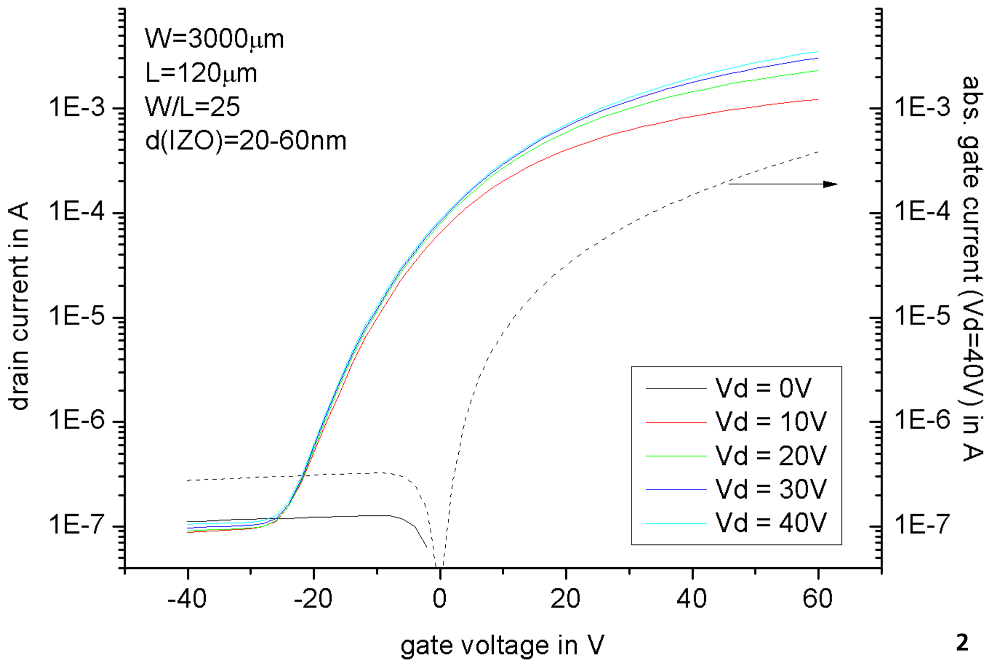
The system capabilities were demonstrated by the areal deposition of semiconducting layers for application in thin-film transistors (TFTs, fig. 2). The device parameters were optimized involving the overall process chain:

- selection of chemistry,
- precursor synthesis,
- spray processing, and
- post-treatment.

The performance of sprayed devices can compete with pixel driver TFTs from vacuum-based amorphous silicon layers commonly used in display technology. Thus, the technique offers a low-cost and easily scalable alternative for the processing of driver electronics.

The encouraging electrical properties indicate a high layer quality with respect to stoichiometry, morphology, and defect levels. However, thin-film transistors are just a small fraction of possible applications for the process. By proper tailoring of starting chemicals, low-cost protection and encapsulation layers, conductive coatings, complex layer stacks (e.g. for chemical surface sensing), and additional functionalities beyond these can be realized.

1 *Automated spray coating equipment for metal-oxide deposition.*



2 *Transfer characteristics of a thin-film transistor based on a spray-coated mixed metal oxide semiconductor layer.*

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POWER ELECTRONIC SYSTEMS

Content

Focal Areas of Research and Development, Trends, and Potentials

2011 was another very successful year for the Power Electronics department. For the first time, the staff exceeded the number of 40, respectively 80 including students. Once again, we achieved an excellent economic result with an industry contribution well above 30 percent. Four colleagues received their PhD, among them two of our working group leaders.

Several EC projects started during the year: SuperLIB, ESTRELIA, and RELY. These projects are focusing on battery and reliability issues. KAIROS, a project funded by the Federal Ministry of Education and Research (BMBF), could also be launched in 2011.

From 14th to 16th February 2011, the second "DRIVE-E Academy" a joint initiative of the Federal Ministry of Education and Research (BMBF) and the "Fraunhofer-Gesellschaft" took place in the Fraunhofer Forum in Berlin. Sixty, mostly correspondingly educated students from all over Germany experienced a week under the thematic banner of e-mobility with professional lectures of well-known speakers, excursions, and the award ceremony for the "DRIVE-E Students' Awards".

The new working group "Drives and Mechatronics" under the direction of Dipl.-Ing. Maximilian Hofmann took up its work on 1st of June. The group is focusing on electric drive solutions for vehicle applications. System integration of power electronics, mechanical and thermal engineering are topics of this group as well as system simulations on vehicle level and the vehicle integration of all the electrical powertrain systems. The latter comprises drives, battery systems and power converters as well as systems for cooling and overall thermal management.

An important step was the launch of the "Energie Campus Nürnberg" (EnCN). Professionals from the University of Erlangen-Nuremberg, the Georg Simon Ohm University of Applied Sciences in Nuremberg (GSO), and the two Fraunhofer institutes IIS and IISB closely cooperate and will share new facilities in Nuremberg. The EnCN is committed to putting into practice the vision of a sustainable power society based on renewable energy. EnCN is a research platform for the development and presentation of a closed renewable energy chain. In the focus of the work packages of the IISB are new solutions for megawatt power electronics, the integration of electrical energy storages in a smart power grid, and comfortable wireless energy interfaces to mobile systems like electric vehicles.

At the end of July, the project "Fraunhofer Systemforschung Elektromobilität" was successfully finalized. The sub-project "Energy generation, distribution and conversion", one of four core projects, was headed by Dr. März from IISB. Several work-packages focused on how to make the power electronic systems necessary in the power train of electric vehicles more robust, compact, and cost- effective. The complete chain of economic value added, from the basic technologies up to power electronic vehicle systems like converters and electrical drives, was considered. The traditional power module was re-thought and designed as an inverter building block with robust user interfaces. The result was a new building block that is more modular, flexible and easy to use, and strongly reduces the engineering expenses at system level. Also responsible for the improved robustness are innovative materials and interconnect technologies developed in the "materials and reliability" group under the lead of Mr. Schletz. The first successful application of the novel inverter building block was a single-wheel axle drive for light-duty commercial vehicles which was developed in another work package of this project. The high-voltage DC/DC converter, also developed in this project by Mr. Popov and Mr. Seliger, found a lot of interest both at the "eCarTec", the leading e-mobility trade show in Munich, and from industrial partners. This ultra-compact converter also was given the Fraunhofer IISB Innovation Award 2011. At "eCarTec", the Schaeffler eWheelDrive received the Bavarian State Award for Electric Mobility 2011 in the category "drive technology and electrical systems". The eWheelDrive is a wheel hub drive that enables the integration of forward-looking vehicle architecture and interior concepts, particularly in electric city vehicles. The system-integrated inverter was completely developed at Fraunhofer IISB. In November, the ENIAC Joint Undertaking announced that the project "Nanoelectronics for an Energy Efficient Electrical Car (E3Car)" received its 2011 Innovation Award. "E3Car" is Europe's largest research project in this field in the last three years. It is executed by 33 partners from 11 European countries with total R&D costs of Euro 44.2 million euros. Together with its industrial partners, the IISB is working on new battery management solutions. The consortium is confident that the overall goal to establish a strong European contribution to the world of battery monitoring ICs is about to be reached with the end of the project in April 2012. The Fraunhofer Innovation Cluster "Electronics for sustainable Energy Use" is also running very successfully. The targeted total industry participation could be reached already in 2011, at about half time of the project. In December, the cluster was evaluated by a number of renowned Fraunhofer internal and external experts. We expect a positive result in early 2012.

Sincere thanks to all of my colleagues in the department and all supporters from industry, politics, and from the institute.

1 *Dr. Martin März, head of department.*

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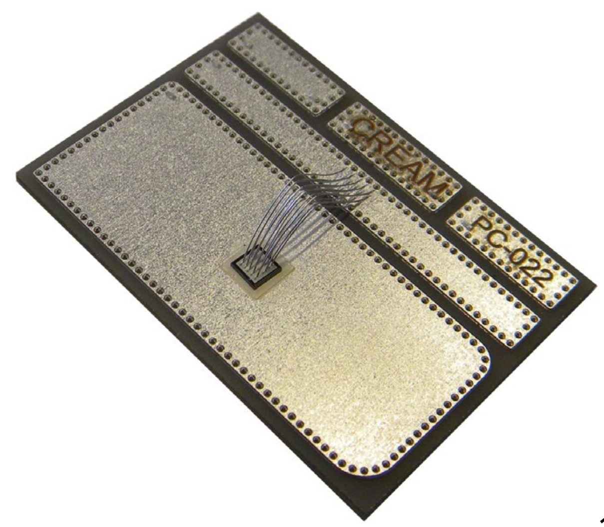
POWER ELECTRONIC SYSTEMS

Technologies for Compact and Reliable Electronics Integrated in Actuators and Motors for Avionic Applications

The goal of the current environmental and economical trends applied to air transport is to eliminate as many hydraulic power sources as possible. Immediate benefits derived from the wider application of electrical power in actuation include higher performances and reliability, benefits of overall weight reduction, easier maintainability, and enhanced safety. For this reason, nine European hightech companies, for example Sagem from France or UAC from Russia, and four research institutes, for example EPFL in Switzerland and TEI-P in Greece, bundle their experiences to perform an ambitious technological research program allowing to develop and validate a number of various emerging sub-components, packaging and motor technologies and to integrate them to a high-performance smart electronic and motor technology platform. For this project, the Fraunhofer IISB investigates new technologies for power electronics assembly with the capability to work in a high-temperature avionic environment.

The reliability of power electronics at high temperatures is limited by the maximum operating temperature of conventional interconnection materials like aluminum wire bonds and tin-based solders. To analyze the reliability of the proposed power module technologies for high-temperature applications, different test vehicles for suitable baseplate materials, substrate, die interconnection and top-side interconnection technologies were built up during the project and different lifetime tests like high-temperature storage, temperature cycling and power cycling were performed at the IISB.

An example technology out of an extensive test matrix consisting of all technologies used for power electronics assembly is the die interconnect technology. The research at Fraunhofer IISB focuses on solder joints made of gold-germanium (AuGe12), zinc-aluminum (ZnAl5), and lead-tin (PbSn5) alloys, as well as die bonding by low-temperature sintering of silver nanoparticles. Thermal aging at 200°C, 250°C and 300°C for up to 1000 hours was performed to analyze thermally activated failure mechanisms. During these tests, the eutectic gold-germanium solder and the sintered silver layer showed excellent mechanical properties. The shear strength of $AuGe_{12}$ solder joints formed on copper surfaces remains almost constant at 25MPa over 1000 hours at 200°C and decreases slightly at 250°C. For samples with a copper metallization, the failure mechanism is given by a brittle fracture directly in the IMC layer and no change with time was observed.



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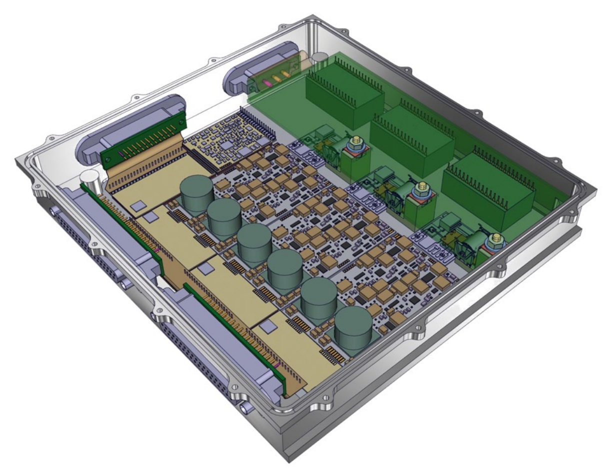
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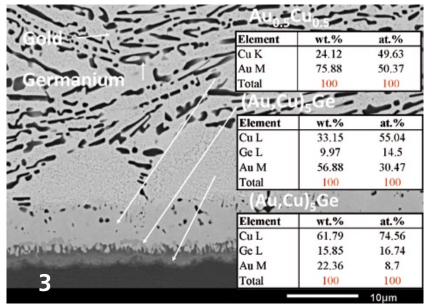
For the sintered joint at 200°C, the shear strength increases with the aging time up to a maximum value of around 50MPa and stays quite constant for up to 1000 hours. At 250°C, constant values of 40MPa of the shear strength with increasing aging time could be observed. At the initial state, the failure occurred within the sintered layer / galvanic layer interface. With increasing aging time, the position of the fracture changed towards the sintered layer itself resulting in a coarse fracture surface on the chip and the substrate side.

During the power cycling tests, the silver sintering technology for the die attach turned out to set a new benchmark regarding the lifetime at high temperatures. While conventional power modules with a 375µm aluminum bond-wire top-side interconnection and a solder layer for the die attach feature a number of cycles to failure of around 13.000 at a temperature swing of 130K and a cycle period of 30s, the sintered silver layer shows a up to 15 times higher lifetime depending on the substrate material.

All investigations performed at IISB showed that with increasing application temperature the selection of materials and processes for the power module assembly becomes more important to guarantee a high reliability and lifetime of the power module especially under additional harsh environmental condition like vibrations, humidity and temperature cycles.

1 Power Cycling test vehicle for high-temperature applications.

2 CAD model of the entire power converter for high temperature applications.



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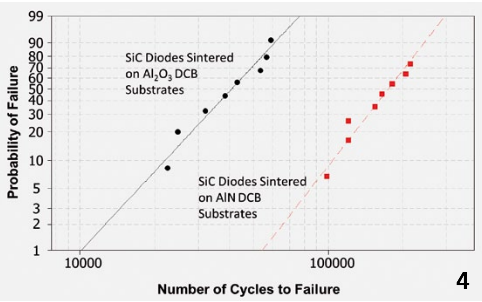

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3 Gold-germanium solder joint on copper after 1000 hours at 250 °C.

4 Power cycling test results of the silver sintering technology on different substrates at 130 K temperature swing.

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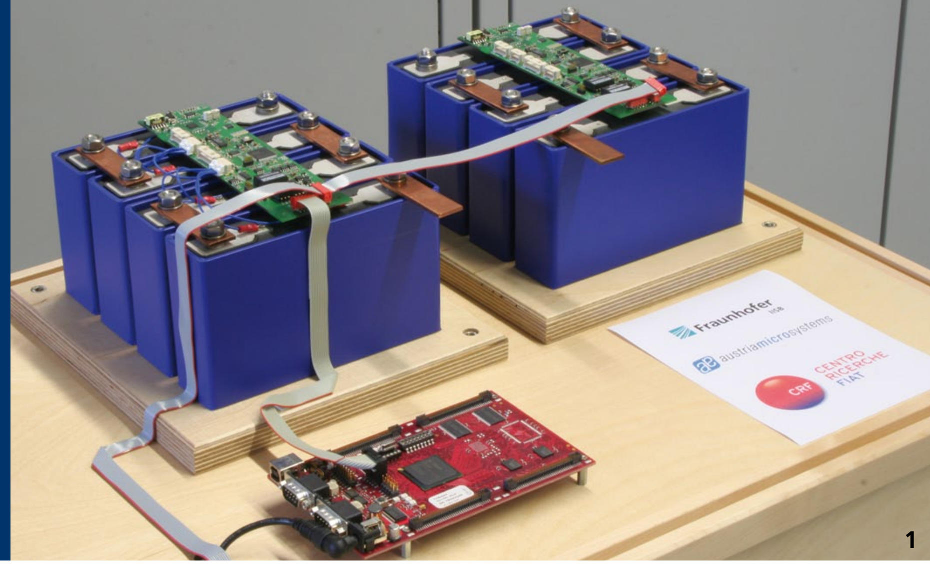

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First Battery Monitoring System with Integrated Active Cell Balancing and Redistribution

In November 2011, the ENIAC "E3CAR" project was honored with the ENIAC Innovation Award. One of the innovative highlights in this project is the development (austriamicrosystems) and implementation (Fraunhofer IISB) of the first battery management IC with integrated active cell balancing using redistribution. Active cell balancing with redistribution means that during the cell equalization process excessive energy is no longer dissipated as heat, but redistributed to support less charged battery cells.

There is no general rule of how to integrate a battery system that applies to all cases. Instead, this article briefly describes an example derived from the experience gained during the "E3Car" project based on the specifications given by CRF (Centro Ricerche Fiat).

The battery system uses a series connection of 96 Li-ion cells with 50Ah capacity in order to reach the required voltage levels of up to 400 V. The cells are divided into groups of four cells: these groups are called modules. The battery pack consists of 24 modules, each including a controller for monitoring and balancing the cells. Figure 1 shows the diagram of such a battery system.

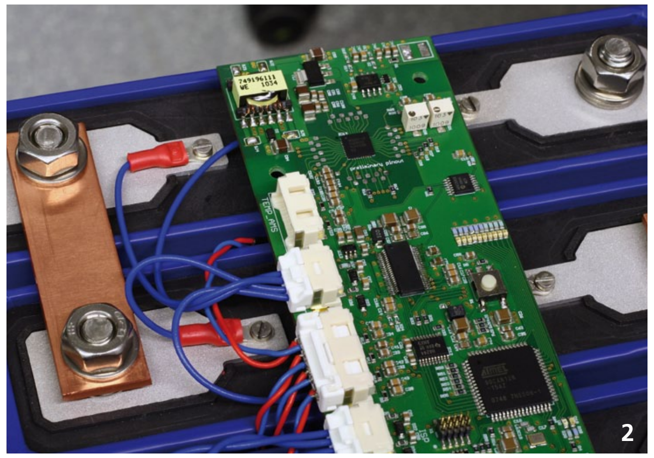
Besides the battery modules with the battery monitoring, the battery system includes the battery management system (BMS). Its role is to acquire data from the battery monitoring circuits and the current sensor, calculate battery parameters like the state of charge (SOC), the state of health (SOH) and the state of function (SOF), communicate with the vehicle control system, operate power switches and control battery cooling and heating subsystems.

The battery management system and the battery monitoring circuits communicate via a CAN bus. The centerpiece of the monitoring circuit is the battery monitoring integrated circuit (IC). In this case, the newly developed AS8505 by "austriamicrosystems" was used. It is the first IC that features an integrated active cell balancing method using redistribution. It is able to support cells with a voltage below a certain threshold value with energy taken from the other cells in a module. The energy is redistributed instead of discharging cells with a higher voltage over a resistive bypass.

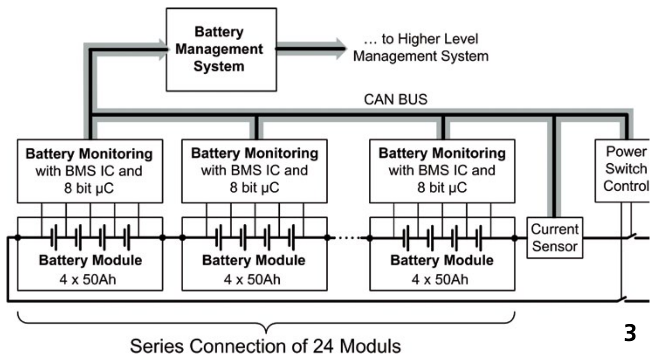
Cell voltage measurement board using the active balancing IC can be seen in figure 2. In the beginning, cell 1 has a slightly higher voltage level than the other cells. The cells with lower voltage are receiving charge pulses, thus the cell voltages are being equalized over time. This is a rather slow process. In an electric vehicle application, the balancing action is done during the time in which the vehicle is not used for driving, i.e. when it is parked. This way, it is possible to maintain a balanced battery stack, even with a relatively low balancing current, which is a prerequisite for integration into a single chip.

A live-demonstrator set-up of the core battery system consisting of battery monitoring and management is shown in figure 1. In the front, the battery management circuit can be seen. In the back, two modules with their monitoring circuit are shown.

1 *Core battery system with battery management circuit in the front and two battery modules in the back.*



2 *Cell voltage measurement board with active balancing IC.*



3 *Battery system overview.*

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Content

Charging Electric Vehicles – From On-board Solutions to Inductive Charging

Every battery electric vehicle needs a charging device to charge its internal lithium-ion battery with energy. The charger's major task is to convert the AC grid voltage to a suitable voltage level the battery needs. First, it seems obvious to use a rather simple unidirectional on-board battery charger with one or two converter stages for this purpose. But a closer look at bidirectional charger topologies reveals their decisive advantages.

In addition to just charge the vehicle's battery, it is possible to feed energy back into the national grid with a bidirectional on-board charging device. With a view to future developments in energy use and environmentally friendly generation of energy, this operating mode will gain in importance. As a result of the increasing number of renewable energy sources and their strongly varying power generation, a destabilization of the national grid occurs. The energy storage capability in future electric vehicles offers the remedy to counter the upcoming problems. These smart and mobile energy storages can be used to enhance grid quality. With a sufficiently high number of electric vehicles, even grid stabilization and feed-back of reactive power is possible. As an additional benefit, the realization of the charger using a bidirectional DC-DC converter allows the implementation of a 230 V on-board power socket, e.g. to charge a notebook or other devices during a journey.

Taking a closer look on possible topologies for bidirectional converters, a topology with three converter stages emerges as a most benefiting alternative. With this kind of topology, a wide - range DC input can be realized supporting a multitude of battery types and stack configurations.

In the context of the project "FSEM – Fraunhofer Systemforschung Elektromobilität", a 2 kW version of the above-mentioned bidirectional on-board charger was developed and tested in the all-electric test vehicle "Frecc0".

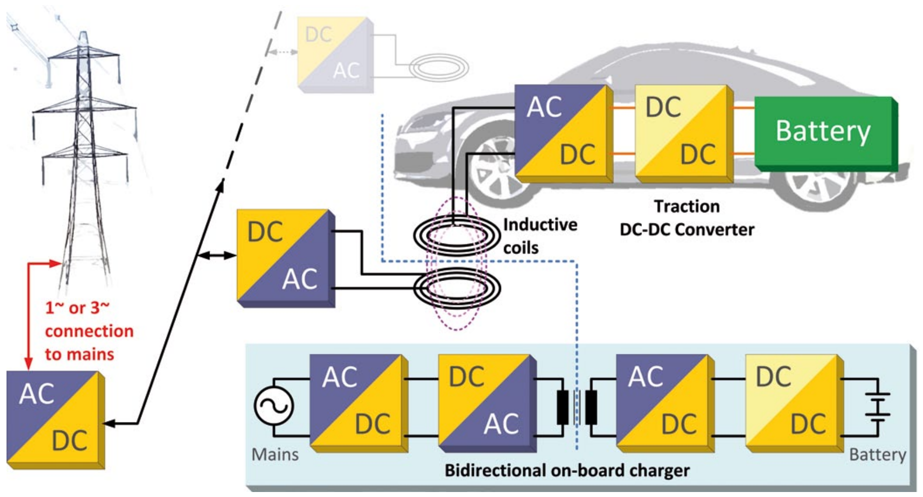
Beyond that, the three-converter topology of the on-board charger also significantly supports the further trend away from a conductive towards an inductive charging process for electric vehicles. The second power electronic converter which realizes the galvanic isolation in the on-board charger provides an excellent hyphenation point for the power electronic components between the vehicle and the charging point. Based on the predevelopment of the bidirectional on-board charger, the design of an inductive charging connection can benefit from the previous results.

An evident starting point is to remove the power electronics connected to the vehicle's battery and the part connected to the grid along the galvanic isolation of the second converter. Hence, the power electronic converter connected to the grid can be implemented as a highly efficient bidirectional AC-DC converter supplying or sinking energy to an inductive parking space. This configuration increases in efficiency, if the AC-DC converter supports several parking spaces instead of just one.

In the electric vehicle, the existing traction DC-DC converter between battery and drive inverter takes over the task of the third power-electronic converter of the on-board charger which realizes the wide-range DC input for the battery. No additional hardware has to be implemented in the vehicle and so the overall weight can be further decreased.

Finally, the inductive connection between vehicle and battery-charging station derives from the original second power converter with galvanic isolation. After removal of the transformer core and enlargement of the transformer windings, one winding will be mounted under the vehicle floor and the other on the road surface. Depending on the energy flow direction, either the coil on the vehicle side or that on the surface side acts as transmitter coil.

The proposed concept of inductive charging will be evaluated in the project "EnCN – Energy Campus Nuremberg" within the sub-project "Net".



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1 *Inductive charging concept for electric vehicles.*

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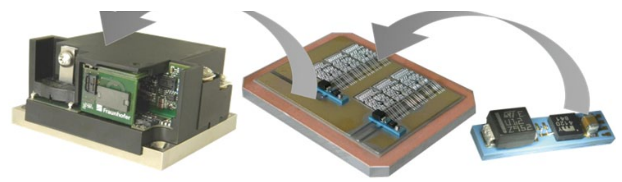

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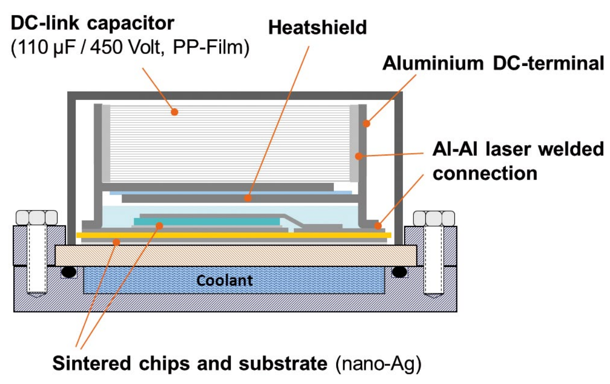

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Modular Power Electronic for Intelligent e-Drives

Within the project "Fraunhofer Systemforschung Elektromobilität" (FSEM), a new design for power modules for the use in hybrid and electric vehicles was developed.

Many of the weakpoints of today's solutions regarding interfaces, constraints for the overall system design, the assembly effort and reliability could be eliminated. The result was the realization and testing of a modular 'inverter building block' shown in figure..

State-of-the-art inverter designs have, for example, an interface between the powermodules and the DC-link capacitor. Constructional constraints regarding the component placement can lead to a high impedance of the commutating cell, especially for integrated drive solutions. The placement of the DC-link film capacitor in the 'inverter building block' leads to a high switching performance of the module, independent of the overall 3D inverter design. This provides also improvements in the fields of robustness (overvoltage margin), EMC behavior and energy efficiency (reduction of switching losses). The gate driver and the current sensor are also integrated in the module. A LTCC device with integrated gate resistors and the power stage of the gate driver is directly soldered on the well-cooled DAB substrate (direct aluminum bonding). This reduces parasitic effects and thermal hot spots.

Integrating power electronic components into mechanical drives leads to a higher level of thermal and mechanical stress compared to stand-alone solutions. To reduce the thermo-mechanical stress within the module, an all-aluminum material concept was used. Innovative joining technologies, like laser welding of the aluminum terminals with the DAB substrate and double-sided nano-silver sintering of the semiconductor devices, were investigated. Power cycling and passive temperature cycling tests have shown a significant improvement of the number of cycles before failure compared to standard technology.

The modular design of the 'inverter building block' allows the use in a variety of drive and motor configurations (e.g. in single or double motor set-ups). A first test of the design was carried out in an axle drive system that was developed in the same project.

The developed axle drive unit includes two mechanically independent permanent magnet synchronous motors (PMSM) with reduction gear (7:1). Each motor has a peak power of 80 kW and a continuous power of 30 kW. The maximum torque per wheel is 2000 Nm. The chosen 'off-axis' concept allows a flexible use in a variety of vehicle concepts, for example in small commercial vans, buses or sports cars.

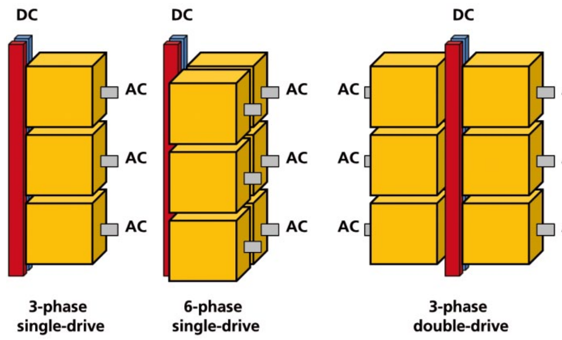
Six 'inverter building blocks' are used to realize the double inverter for the drive unit with a nominal phase current of 350 Arms and a nominal DC-link voltage of 400 V. The two independent field-oriented control algorithms are implemented on a central control board with "TriCoreTM" processor and CAN communication to the superior vehicle control system. This allows an independent torque control for each wheel of the axle. An advanced safety architecture is implemented to meet the "ASIL-D" safety level.

The power-electronic components including the 'inverter building blocks', the controller and the DC busbars are completely integrated into the electric drive. This reduces the required space, the costs and also leads to an improved EMC behavior. A direct connection of the motor AC cables without additional connectors and the common use of one cooling circuit for the two electric machines and the power electronics reduce, amongst other things, the material and production costs.

The development of the axle drive unit was carried out at Fraunhofer IISB. The research work of the power module was done in cooperation with the Fraunhofer institutes IFAM, IKTS, ILT, IMS and ISIT.

1 *Modular 'inverter building block' (module, DAB substrate, LTCC).*

2 *Sectional view of 'inverter building block'.*



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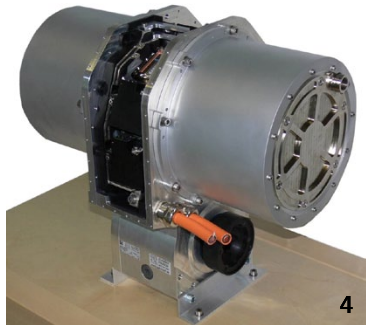

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3 *Possible inverter configurations.*

4 *Intelligent e-Drive (2 x 80 kW-Peak) with integrated double inverter.*

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Selected News

AWARDS AND PRIZES

The research and development prizes of the IISB were awarded again on December 20, 2011. These awards are given by the board of directors of the institute to employees who have made exceptional contributions to the success and further development of the IISB. The director of the institute, Lothar Frey, presented the awards at a ceremony. This year, the prizes went to Jordan Popov and Bernd Seliger for developing an innovative voltage transformer concept as well as the to the „Laue-Scanner" team, consisting of Dr. Elke Meißner, Matthias Trempa, Dr. Christian Reimann, Toni Lehmann and Tobias Geiger, for developing a method for fast microstructure analysis of crystalline silicon for photovoltaics.

Feng Shao, an employee of the Department of Technology Simulation at the Fraunhofer Institute for Integrated Systems and Device Technology IISB, received the "Student Award 2011" of the Erlangen Graduate School in Advanced Optical Technologies (SAOT) of the University of Erlangen-Nuremberg in the category "Optical Material Processing". The prize, which is worth 1000 €, was awarded to Shao in recognition of his scientific results published in the article "Mask-Topography-Induced Phase Effects and Wave Aberrations in Optical and Extreme Ultraviolet Lithography", which appeared in the "Journal of Vacuum Science and Technology".

Junior researcher Ludwig Stockmeier was awarded the Georg Kurlbaum Prize for his diploma thesis on the defect inventory in crystalline solar silicon, which he wrote at the Fraunhofer IISB in Erlangen. The results of his research make it possible to produce better-quality silicon crystals with an inexpensive method and thus realize solar cells with greater efficiency. Since this helps to preserve and improve the environment – entirely in the spirit of the Kurlbaum Foundation, Ludwig Stockmeier was awarded the 2011 Georg Kurlbaum Prize in the category of Environment / Energy.

Markus Billmann and Dirk Malipaard of the Fraunhofer IISB as well as Andreas Zenkner (Siemens AG, Nuremberg) and Christoph Blösch (Blösch design office, Bubenreuth) received the Innovation Award for Microelectronics from Förderkreis für die Mikroelektronik e.V. ("Sponsorship Association for Microelectronics"). The innovation award for 2011 was to recognize a development in the field of electronics for energy supplies. The award recipients were honored for their innovative inverter cell design, which can considerably improve the current stability in medium- and high-voltage applications. This is important for the use of locally produced regenerative energies.

1 *Ludwig Stockmeier with the Georg Kurlbaum Prize 2011 in the category of Environment / Energy at his crystal growth furnace in a crystal growing laboratory at Fraunhofer IISB.*
Image: Fraunhofer IISB

2 *From left to right: Tobias Geiger, Dr. Elke Meissner, Matthias Trempa and Dr. Christian Reimann of Fraunhofer IISB as well as Dipl.-Ing. Toni Lehmann of Fraunhofer THM with the Research and Development Award 2011 of Fraunhofer IISB.*
Image: Fraunhofer IISB

3 *M.Sc. Feng Shao of Fraunhofer IISB at his workplace during the simulation of complex optical processes.*
Image: Fraunhofer IISB

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The innovation award was presented along with the Youth Prize for Microelectronics by the chairman of the sponsorship association, Dr. Dietrich Ernst, as part of the "Power Electronics" lecture series at the Fraunhofer Institute IISB in Erlangen.

AWARDS FOR INNOVATIVE IDEAS IN ELECTROMOBILITY: DRIVE-E student prizes in 2011

On Tuesday, February 15, 2011, the DRIVE-E student awards for innovations in the field of electromobility were presented at a ceremony at Umspannwerk Ost in Berlin, Germany. Dr. Georg Schütte, State Secretary in the Federal Ministry for Education and Research (BMBF) and Prof. Ulrich Buller, Research Director at the Fraunhofer-Gesellschaft, handed out the awards to the five recipients. In 2011, the DRIVE-E student awards were bestowed in two different categories for the first time. In the category „Student research projects and bachelor's theses", a student research project on the driving dynamics of vehicles with wheel hub motors by Marcus Walter from TU Kaiserslautern University was selected for the first prize. The second prize went to Oliver Wallscheid from the University of Paderborn for his bachelor's thesis on the improvement of electric motors. In the category „Diploma and master's theses", Mareike Hübner and Michael Reiter, both from RWTH Aachen University, shared the first prize for their diploma theses on the development of a drive inverter for electric drives. The second prize went to Peter Keil from TU München University for his diploma thesis on the development of a computer model for lithium-ion batteries. The first prize was endowed with € 5,000 (or € 3,500 per person if the prize was shared), and for the second prize the prize winners received € 2,000 each.

The DRIVE-E student award is given for outstanding student projects at German universities or advanced technical colleges that make innovative contributions to the further development of electromobility. Students and graduates in the fields of electrical engineering, mechanical engineering, mechatronics or related subject areas can participate.

DRIVE-E ACADEMY 2011: A meeting of young electromobility specialists in Berlin

Electromobility from A to Z awaited the participants of the DRIVE-E Academy, which took place from February 14 to 18, 2011 at the Fraunhofer Forum on Electromobility. Around 50 selected students from all over Germany received the opportunity to learn about current developments in the field of electromobility, establish networks and gain practical experience in the future-oriented technology of electromobility over a period of one week. The program included technical pre-

1 Presentation of the DRIVE-E Award 2011: BMBF State Secretary Dr. Georg Schütte (back right) and Fraunhofer Chairman Prof. Ulrich Buller (back left) presented the awards to Mareike Hübner and Michael Reiter (back center), Marcus Walter (front center), Peter Keil (front left) and Oliver Wallscheid (front right).
Image: BMBF / Fraunhofer / Leo Seidel

2 The participants in the DRIVE-E Academy 2011 in Berlin.
Image: BMBF / Fraunhofer / Leo Seidel

1

1 *Prof. Joszef Gyulai of the Hungarian Academy of Sciences (right) congratulates his long-standing scientific colleague Prof. Ryssel on his 70th birthday.*
Image: Fraunhofer IISB

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sentations, discussion groups and workshops with experts from renowned research institutions and industrial companies, excursions to automobile and electric vehicle manufacturers as well as joint social events.

In addition to the DRIVE-E Student Award, the annual holiday course is the second main component of the DRIVE-E program to introduce young people to the subject of electromobility and show them career paths in this forward-looking sector.

DRIVE-E started in 2009 as a joint initiative of the Federal Ministry of Education and Research (BMBF) and the Fraunhofer-Gesellschaft to promote young researchers in electromobility. On the part of the Fraunhofer-Gesellschaft, the Fraunhofer IISB is the initiator and organizer of the DRIVE-E events. The BMBF has been investing considerable funds in the promotion of leading-edge research subjects for many years, e.g. to support the development of the automobile industry in Germany in the area of electromobility.

Further information can be found at www.drive-e.org.

TECHNOLOGY SIMULATION AS AN INDISPENSIBLE TOOL – 2011 Annual Conference of the IISB

The rapid development in microelectronics is only possible with massive assistance from the simulation of processes and new components. The IISB showed how this is done at their annual conference on December 9, 2011 in Erlangen, Germany. In addition to producing increasingly efficient i.e. faster and smaller components and circuits, central challenges include reducing production costs as well as improving the reliability and lifetime of electronic components. Since current semiconductor components manufactured with nanotechnology are increasingly approaching physical limits, it is necessary to precisely understand the basic processes to find optimum solutions.

This is where semiconductor process and component simulation comes in: researchers use physical models to investigate and optimize the production and characteristics of semiconductor components on the computer. As a result, simulation not only helps to greatly reduce development times and costs but also creates new possibilities for the comprehensive investigation, development and optimization of semiconductor processes and components.

Since the IISB was founded in 1985, it has been active in the field of semiconductor process simulation and has decisively shaped its development in Europe. The institute cooperates with numerous partners from industry and research. At the annual conference, the IISB introduced examples of the development and application of semiconductor process and component simulation, together with partners from industry and research. The program was rounded off by demonstrations of software simulation.

A high point occurred at the conclusion of the event: on the occasion of the 70th birthday of the former director of the IISB, Prof. Heiner Ryssel, who also initiated the simulation of semiconductor processes in Germany in the 1970's, Dr. Jürgen Lorenz, director of the Department of Technology Simulation at the IISB, gave an overview of the development in this research field at the institute. The annual conference came to a close at the Fraunhofer cafeteria with a cozy get-together featuring local Franconian specialties.

Material from the annual conference can be found on our Internet site at www.iisb.fraunhofer.de/techsim.

THE SMALLEST STRUCTURES FOR ELECTRONICS – Fraunhofer lithography workshop combines international expertise

For the ninth time, lithography experts from all over the world accepted the invitation of the IISB to the "Fraunhofer IISB Lithography Simulation Workshop". This specialist conference focusing on modeling is aimed at an international public from industry and research and places particular emphasis on practical applications.

The miniaturization in microelectronics continuously produces new technological challenges for lithography. Computer simulations are an indispensable tool for answering questions that would be too expensive, time-consuming or technically impossible to clarify experimentally.

The lithography workshop from September 15 – 17, 2011 focused on the latest research activities and future developments in the field of lithography and lithography simulation as well as the limits and necessary expansion of current simulation models. Topics included physical modeling, numerical techniques as well as devices and processes in semiconductor manufacturing. In addition to questions concerning EUV (extreme ultraviolet) lithography, photoresist exposure processes that have not yet been completely clarified in detail also provided material for discussion. Other key topics were lithography for micro- and nanooptics as well as alternative applications of lithography simulations.

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The workshop was held by the lithography simulation workgroup of the IISB, as every year. The conference, which was filled to the very last place, is very popular among participants from America, Asia and Europe. The workshop attractively combines a technical orientation and an exceptional environment. The venue is traditionally located in the delightful countryside near Hersbruck, Germany in the Franconian Alb mountains, and social aspects are an integral part of the program. This special atmosphere offers the best possibilities for intensive and creative discussions as well as personal exchange.

ELECTRIC DRIVES GET ENERGIZED – A new group at the IISB for drive research

Efficient, compact, robust, reliable, highly integrated, as well as optimized in terms of raw materials and costs – the list of requirements for electric drives is long, especially in the automotive sector, and presents automobile manufacturers and suppliers with great challenges in view of the global race for future electromobility markets. The IISB has been a partner of the automobile industry in this field for around a decade and has repeatedly set standards and made pioneering contributions with their developments in system integration. With the creation of a new workgroup, the IISB is further expanding its research focus in the field of power electronics and drive technology for electric vehicles.

The main working area of the new workgroup „Drive Technology and Mechatronics“, headed by qualified engineer Maximilian Hofmann, is the development of electric drive solutions for vehicle applications. This includes electric motors with mechatronically highly integrated drive inverters, the development of control electronics, driver circuits and control algorithms, the driving-cycle-based design of the all-electric drive train as well as general CAD models and simulations. The institute can rely on the extensive equipment in its test center for electric vehicles.

The new „Drive Technology and Mechatronics“ workgroup of the IISB began its work in June 2011 and supplements the previous activities of the „Vehicle Systems“ workgroup of Dr. Bernd Eckardt. This considerably expands the spectrum of expertise concerning the electric drive train even more, further expanding electromobility research in the metropolitan region of Nuremberg, Germany.

1 *Section view of a wheel-hub-motor with integrated inverter.*
Image: Fraunhofer IISB

2 *The participants in the "9th Fraunhofer IISB Lithography Simulation Workshop" 2011 in Hersbruck.*
Image: Fraunhofer IISB

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STARTING SIGNAL FOR THE ENERGIE CAMPUS NÜRNBERG

With the signature of the cooperation agreement by the partners and the granting of initial funding approval by Bavarian Minister-President Horst Seehofer, Minister for Economic Affairs Martin Zeil and Minister of Science Dr. Wolfgang Heubisch on May 10, 2011, the Energie Campus Nürnberg (Energy Campus Nuremberg – EnCN) was officially started.

At the EnCN, the University of Erlangen-Nuremberg (FAU), the University of Applied Sciences Nuremberg (OHM), the Fraunhofer Institutes IIS and IISB as well as the Bavarian Center for Applied Energy Research (ZAE) work together in a cooperation that is unique in Germany. The city of Nuremberg, the Chamber of Commerce and Industry and the Chamber of Crafts as well as the industrial partners of the research institutions are also closely involved.

As part of the structural program for the cities of Nuremberg and Fürth, the Free State of Bavaria is providing 50 million EUR to establish and expand the research platform in the first five years. In June 2011, the first four research areas of the EnCN started work and six more will follow in the coming months.

The four areas that are already functional also include the EnCN focus „NET – Electric Grids" – the largest support package in the Energie Campus and the field of activity of both Fraunhofer Institutes. NET answers central questions regarding the reorganization of power grids and thus our future power supply. Topics include energy flow control, interfaces and storage solutions for future power grids and appropriate information and communications technologies. The IISB contributes to this particularly with their expertise in power electronics and system integration.

The kick-off meeting for this part of the EnCN took place on June 16, 2011 in Nuremberg. Here, the details for the joint action were coordinated among the involved research institutions IIS, IISB, FAU, and OHM.

LECTURE SERIES OF THE FRAUNHOFER INNOVATION CLUSTER „ELECTRONICS FOR SUSTAINABLE ENERGY USE"

Once again, the „Power Electronics" public lecture series of the Fraunhofer innovation cluster „Electronics for Sustainable Energy Use" was very well received. The lecture series is organized by the Fraunhofer IISB together with the Bavarian Cluster „Power Electronics" and deals with current topics in the field of modern and efficient electronics. In 2011, the key topics of „SiC Power Semiconductors", „Electric Traction Drives", „Solar Energy Supply", „High-Performance Capacitors", „Multi-Level Converters", „Inductive Devices", „Electromobility", „Electrical Energy Supply" as well as „Electric Traction" were dealt with. In addition to lectures by experts from universities, research and industry, current technical topics were discussed and contacts were intensified among local people involved in power electronics. The exchange of ideas was also promoted and innovations were initiated. The lecture series is an important element in the efforts of the innovation cluster to link science and industry, and its great resonance among the specialists exceeded all expectations.

The series will continue in 2012; current information can be found on the Internet at www.iisb.fraunhofer.de/innocluster.

EXCELLENT GRADES FOR ERLANGEN ELECTRONICS RESEARCH

In the scope of a nationwide research rating of the Council of Science and Humanities in the field of electrical engineering and information technology, the IISB received consistently positive assessments.

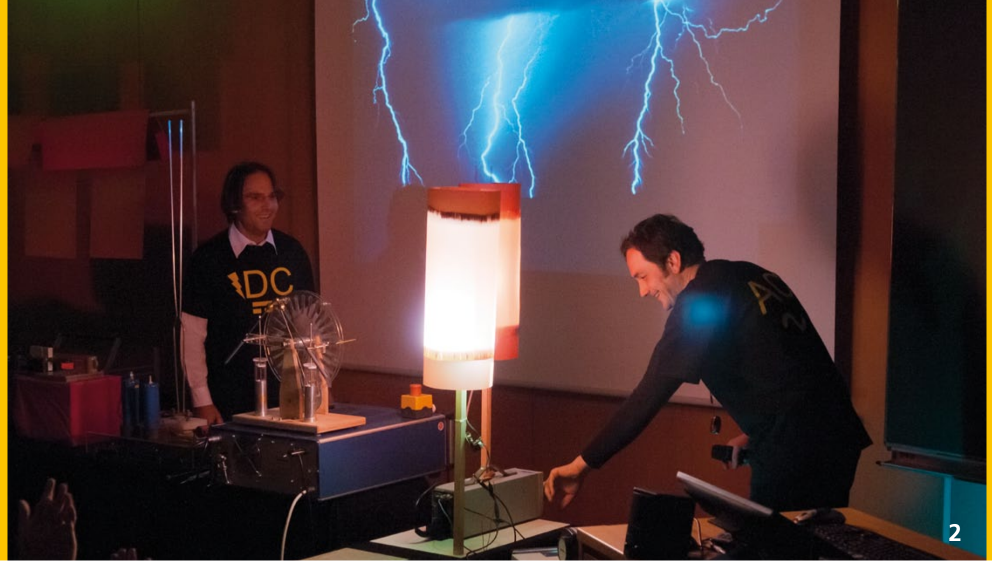
For example, the research quality in the field of "electronics and microsystems" as well as the research performance in relation to employed staff ("efficiency" criterion) were rated "very good/good", the promotion of young researchers was "good", and the research activity and visibility ("impact/effectiveness") as well as the transfer of knowledge for economic utilization of the results were even "very good".

Very good grades were also given to the Department of Electrical, Electronic and Communication Engineering of the University of Erlangen-Nuremberg, which also includes the Chair of Electron Devices, led by IISB institute director Prof. Lothar Frey. Particular mention should also be made here to a "very good" research quality in the area of "electronics and microsystems" as well as a "very good" in the promotion of young researchers.

The rating is to aid the research institutions in identifying and classifying their strengths and weaknesses in comparison to their competitors. 31 German universities and 16 non-university institutions were evaluated for this purpose.

The results can be found at www.forschungsrating.de.

1 *Signing of the project co-operation agreement for the EnCN area "Net", from left to right: Dr. Christian Weindl (FAU), Prof. Armin Dietz (OHM), Prof. Albert Heuberger (Fraunhofer IIS), Prof. Robert Weigel (FAU), Prof. Lothar Frey (Fraunhofer IISB), Prof. Robert Fischer (FAU) Image: Fraunhofer IIS / Rida El Ali*



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2011 LONG NIGHT OF SCIENCE AT THE IISB

In cooperation with the Chair for Electron Devices (LEB) of the University of Erlangen-Nuremberg, the IISB opened its doors again to almost 2000 visitors for the Nuremberg-Fürth-Erlangen Long Night of Science on October 22. The wide spectrum of presented activities ranged from growing crystals to a tour of the clean room to electric cars on the test bench and a talk on the topic of "Electrotainment".

Crystals are high-tech materials that are used in almost all fields of electronics. The IISB scientists presented production methods and application areas in a vivid manner using exhibits and posters.

Tours were given of the new test center for electric vehicles of the IISB. This provides a unique infrastructure in which individual components up to entire vehicles can be measured and optimized, e.g. in regard to operation under extreme climate conditions.

The well-received talk on "Electrotainment" explained the basic principles of electricity in an entertaining and interesting way, using colorful and impressive experiments such as glowing cucumbers or wandering lightning bolts.

As always, the tours of the huge clean room of the LEB were particularly in demand during the Long Night. This gave visitors an insight into the highly developed technology and infrastructure that is required to produce nanometer structures.

Further topic areas that the IISB and the LEB presented during the Long Night were "Computer simulation for semiconductor technology", "Printed electronics", "Electronics for sustainable energy use – electronics help to save energy" as well as "Electromobility – from the computer to the street".

The pleasures of the palate were optimally provided for as always by the Fraunhofer cafeteria, e.g. with the "Long Night skewer", which was also very popular this year.

1 *Visitors to the Long Night of Sciences 2011 in the foyer of Fraunhofer IISB. Image: Fraunhofer IISB*

2 *„AC & DC" in action: Stefan Zeltner and Thomas Richter explain the basic principles of electricity with illustrative experiments during the experimental lecture „Electrotainment at the IISB". Image: Fraunhofer IISB*

NAMES AND DATA

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Guest Scientists

Agarwal, M.:
16.05. - 28.07.2011
India
Malaviya National Institute of Technology Jaipur (MNIT)
Ag Backreflectors for thin film solar cells

Andra, R.:
01.07. - 13.07.2011
Romania
Imperial College London
Visuelles programmier
Interface für Lithographie
Simulationssoftware Dr. LiTHO

Bálint, F.:
09.11. - 18.11.2011
Hungary
MFA/KFI Budapest
Messung von ZiO Proben im Rahemen des DAAD-MÖP

Cotrau, V.:
03.10. - 12.10.2011
Hungary
MFA Budapest
Characterization of Gate Stacks by Ellipsometry

Csaba, M.:
21.11. - 24.11.2011
Hungary
MFA/KFI Budapest
Characterization of Gate Stacks by Ellipsometry

Emil, A.:
09.11. - 18.11.2011
Hungary
MFA/KFI Budapest
Messung von ZiO Proben im Rahmen des DAAD-MÖP

Gyorgy, J.:
21.11. - 24.11.2011
Hungary
MFA/KFI Budapest
Characterization of Gate Stacks by Ellipsometry

Gyulai, Prof., J.:
06.12. - 10.12.2011
Hungary
MFA Budapest
Characterization of Gate Stacks by Ellipsometry

Iglesias, V.:
04.02. - 25.04.2011
Spain
Universidad Autonoma de Barcelona (UAB)
Characterization of high dielectric reliability by electrical SPM methods

Janosov, M.:
17.10. - 23.10.2011
Hungary
MFA Budapest
Characterization of Gate Stacks by Ellipsometry

Kerim Tugrul, A.:
01.08. - 26.09.2012
Turkey
Milkent University, Bilkent, Ankara
Kompaktmodelle für nanoskalierte CMOS Transistoren

Kozma, P.:
17.10. - 29.10.2011
Hungary
MFA Budapest
Characterization of Gate Stacks by Ellipsometry

Nemeth, A.:
03.10. - 12.10.2011
Hungary
MFA Budapest
Characterization of Gate Stacks by Ellipsometry

Ory, P. E.:
11.04. - 01.07.2011
France

Ouennoughi, Z.:
01.07. - 31.07.2011
Algeria
University of Ferhat Abbas Sétif
Department de physique Faculté des scienses
Stress and capacitance voltage characteristics of SiC devices

Petrik, Dr., P.:
20.01. - 30.01.2011
25.07. - 31.07.2011
09.11. - 19.11.2011
06.12. - 10.12.2011
Hungary
MFA Budapest
Characterization of Gate Stacks by Ellipsometry

Polgar, O.:
21.11. - 24.11.2011
Hungary
MFA/KFI Budapest
Characterization of Gate Stacks by Ellipsometry

Shruti, J.:
16.05. - 17.07.2011
India
IIT Roorkee
Charakterisierung und Modellierung von Dünnfilmtransistoren

Takai, Prof., M.:
23.03. - 26.03.2011
07.04. - 09.04.2011
Japan
Osaka University

Tanasie, C.:
15.09. - 15.12.2011
Romania
West University of Timisoara
Simulation von Wärme und Stofftransport bei der Czochralski-Kristallzüchtung von Silizium unter Magnetfeldeinfluss

Zeddoug, J.:
11.04. - 01.07.2011
France

Content

Patents

Berwian, P., Friedrich, J.
Verfahren zum Bearbeiten eines Subtrats
Erfindungsmeldung 27.6.2007
DE 10 2007 029 666 A1

Billmann, M., Domes, K.
Umrichtermonitor
Erfindungsmeldung 13.10.2008
EP2238817

Burenkov, A.
An interconnection network between semiconductor structures, integrated circuit and method for transmitting signals
Erfindungsmeldung 20.12.2007
US 2008/0212975 A1

Meissner, E., Birkmann, B.
Method for increasing the conversion of group III metals to group III nitrides in a fused metal containing group III elements
Erfindungsmeldung 4.10.2005
US 2008/0290327 A1

Meissner, E., Müller, G.
Vorrichtung und Verfahren zur Herstellung von Schichten und/oder Kristallen aus Nitriden von Metallen der Gruppe III des PSE
Erfindungsmeldung 12.10.2006
DE 10 2006 048 409 A1

Schwarzmann, H., Berberich, S.
Vorrichtung und Verfahren zum Schalten von elektrischen Signalen und Leistungen
Erfindungsmeldung 12.2.2009
US 2009/0230441 A1

Waller, R., Berberich, S.
Verfahren zur galvanisch getrennten Informations- und Energieübertragung zwischen zwei elektronischen Schaltungseinheiten
Erfindungsanmeldung 30.6.2006
DE 10 2006 032 392 A1

Participation in Commitees

Bauer, A.
- ITG Informationstechnische Gesellschaft im VDE, Fachbereich 8 Mikroelektronik, Fachausschuss 8.1 Festkörpertechnologie, Fachgruppe: Heißprozesse
- Member of the Technical Program Committee of the "40th European Solid-State Device Research Conference" (ESSDERC' 10), Sevilla, Spain, September 13 - 17, 2010
- Member of the Steering Committee of the Workshop of Dielectrics in Microelectronics (WoDiM 2010), Bratislava, Slovakia, June 28 – 30, 2010

Erdmann, A.
- Member of the Program Committee of the "Micro- and Nanoengineering Conference Europe (MNE) 2010", Genoa, Italy, September 2010
- Member of the Program Committee of SPIE Advanced Lithography, San José, USA, February 2010

Erlbacher, T.
- Mitglied im Arbeitskreis „Materialien für nichtflüchtige Speicher" der Deutschen Gesellschaft für Materialkunde

Frey. L.
- Mitglied der Studienkommission Elektrotechnik, Elektronik und Informationstechnik
- Mitglied der Deutschen Physikalischen Gesellschaft
- Mitglied der Böhmischen Physikalischen Gesellschaft
- Member of the Excellence Cluster "Engineering of Advanced Materials" (EAM) der Universität Erlangen-Nürnberg
- Mitglied der Erlangen Graduate School in Advanced Optical Technologies (SAOT)
- Mitglied des wissenschaftlichen Beirats des Leibnitz-Instituts für Innovative Mikroelektronik IHP Frankfurt/Oder

Content

Continuation: Participation in Commitees

- Member of the Evaluation Panel (NT-L) of the Swedish Research Council
- Representative of the Fraunhofer Gesellschaft / Microelectronics Alliance at the European Semiconductor Industry Association (ESIA)
- Nationale Plattform Elektromobilität, AG1
- Wissenschaftlicher Beirat der NaMLab GmbH in Dresden
- Advisory Board, Res. Inst. for Tech. Phys. and Matl. Sci. (MFA), Budapest, Ungarn
- Kerngutachter in der Auswahlkommission „Kooperative Projekte“ der Fraunhofer Gesellschaft mit dem Max-Planck-Institut
- Wissenschaftlicher Beirat der Gesellschaft für Mikro- und Nanoelektronik GMe, Wien, Österreich

Friedrich, J.

- Leiter des Arbeitskreises Massivhalbleiter der „Deutschen Gesellschaft für Kristallwachstum und Kristallzüchtung“ (DGKK)
- Member of the Organisation Committee of the “International Conference on Crystal Growing” (ICCG-17), Warsaw, Poland
- Advisory Committee of 4th International Workshop on Science and Technology of Crystalline Si Solar Cells (CSSC4), Tapei, Taiwan, October 26 – 28, 2010
- Session coordinator “Technologies for Growth of Bulk Wide-bandgap Semiconductors” 5th International Workshop on Crystal Growth Technology, Berlin, Germany, June 26 - 30, 2011
- Reviewer for the „Journal of Crystal Growth“, Applied Physical Letters

Häublein, V.

- Mitglied der GMM-Fachgrppe 1.2.2.
- Mitglied der ITG-Fachgruppe 8.1.1. „Ionenimplantation“

Jank, M.

- Mitglied im Arbeitskreis „Materialien für nichtflüchtige Speicher“ der Deutschen Gesellschaft für Materialkunde

Lorenz, J.

- Chairman of the Modeling and Simulation International Working Group (ITWG) of the ITRS (International Technology Roadmap for Semiconductors)
- Member of the Technical Committee of the “2010 International Conference on Simulation of Semiconductor Processes and Devices” (SISPAD 2010), Bologna, Italy, September 4 - 9, 2010
- Member of the Program Committee of the “40th European Solid-State Device Research Conference” (ESSDERC 2010): Sub-Committee “Process and Device Simulation“, Sevilla, Spain, September 12 - 17, 2010
- Member of the Electrochemical Society
- Member of the Institute of Electrical and Electronics Engineers (IEEE)

März, M.

- Wissenschaftlicher Beirat „Bayerisches Cluster Leistungselektronik“
- Wissenschaftlicher Beirat „Conference on Integrated Power Systems“ CIPS
- Wissenschaftlicher Beirat „Automotive Power Electronics Conference“ APE, Paris
- Stellvertretender Vorsitzender des Fachbereichs Q1 „Leistungselektronik und Systemintegration“ im VDE ETG
- VDE/ETG Fachausschuss A1-Antriebstechnik
- Lenkungskreis „Fraunhofer Systemforschung Elektromobilität“
- Fachbeirat im „Forum Elektromobilität e.V.“
- Nationale Plattform Elektromobilität, AG1
- Center for Transportation & Logistics Neuer Adler e.V. (CNA), Steuerungskreis Automotive
- DRIVE-E Akademie, Gutachterkreis und Programmkomitee

Meissner, E.

- Member of the International Steering Committee for Bulk Nitride Semiconductors
- Member of the Publication Committee IWBNS-7
- Reviewer für Journal of Crystal Growth
- Reviewer für Journal of Materials Chemistry and Physics
- Mentorin im ARIADNE Mentoring Programm der Technischen Fakultät der FAU

Nutsch, A.

- Chair of the GMM Yield Enhancement User Group
- Co-chair of the Yield Enhancement International Working Group (ITWG) of the ITRS (International Technology Roadmap for Semiconductors)
- Member of the Defect Detection and Characterisation Working Group (DDC) of the ITRS (International Technology Roadmap for Semiconductors)

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Öchsner, R.

- Member of the "Factory Integration Working Group (FITWG)" of the "International Technology Roadmap for Semiconductors (ITRS)"
- Member of Semicon Europe Semiconductor Technology Programs Committee (STC)
- Member of the Steering Committee European 450mm Equipment & Materials Initiative: EEMI 450
- Mitglied im Kernteam Spitzencluster Automation Valley
- Member of the Advisory Committee "online educa", International Conference on Technology Supported Training and Learning
- Member of SEMI European Equipment Automation Committee
- Member of SEMI Task Force: Equipment Productivity Metrics Task Force
- Member of SEMI Task Force: Process Control Systems (PCS)
- Member of SEMI Task Force: Data Quality

Otto, M.

- Mitglied des Normenausschusses für Materialprüfung (NMP) des DIN Deutschen Instituts für Normung e.V.
- Mitglied des Arbeitsausschusses NA 062-02-21 AA „Prüfung von Prozesschemikalien für die Halbleitertechnologie" des Normenausschusses für Materialprüfung (NMP) des DIN Deutschen Instituts für Normung e.V
- Mitglied der "Yield Enhancement International Working Group" und der "Wafer Environment and Contamination Control Group" der ITRS (International Technology Roadmap for Semiconductors) und Mitarbeiter an der YE7 Tabelle der Roadmap für 2010
- Head of the SEMI International Environmental Contamination Control Task Force of the SEMI Equipment Automation Committee
- Mitarbeit an VDI 2083 Blatt 16.2 „Mini-Environments" (Neueinstellungen) des VDI

Pichler, P.

- Member of the Board of Delegates of the European Materials Research Society (E-MRS)

Pfitzner, L.

- Honorarprofessor an der Universität Erlangen-Nürnberg, Fachbereich Elektrotechnik
- Chairman of the „Yield Enhancement Working Group" (ITWG) of the ITRS (International Technology Roadmap for Semiconductors)
- Chairman of the Program Committee for the „10th Annual European AEC/APC Conference 2010", Catania, Italy, 28. - 30. April, 2010
- Member of the Program Committee ISSM 2010 (IEEE „International Symposium on Semiconductor Manufacturing Conference"), Tokyo, Japan, 18. - 20. October, 2010
- Mitglied der VDE/VDI Gesellschaft für Mikroelektronik, Mikro- und Feinwerktechnik, Fachbereich „Halbleitertechnologie und Halbleiterfertigung", Leiter des Fachausschusses „Produktion und Fertigungsgeräte"
- Mitglied der VDE/VDI Gesellschaft für Mikroelektronik, Mikro- und Feinwerktechnik, Fachbereich „Halbleitertechnologie und Halbleiterfertigung", Leiter der Fachgruppe 1.1 „Geräte und Materialien"
- Co-chair of the SEMI Task Force „Environmental Contamination Control"
- Co-chair of the Standardization Committee „Equipment Automation Standards Committee" of SEMI
- Member of the „Global Committee" of SEMI
- Member of the European Planning Group for 450 mm Technology

Roeder, G.

- Head of the SEMI Integrated Measurement Task Force Europa
- Koordinator der VDE/VDI-GMM-Fachgruppe 1.2.3 „Abscheide- und Ätzverfahren"

Rommel, M.

- Koordinator der VDE/VDI-GMM-Fachgruppe 1.2.6 „Prozesskontrolle, Inspektion & Analytik"

Roth, A.

- ZVEI Arbeitskreis „Robustness Validation - Hochtemperatur- u. Leistungselektronik"

Ryssel, H.

- International Committee of the Conference "Ion Implantation Technology" (IIT). The conference takes place biannually alternatingly in Europe, the USA, and East Asia.
- Mitglied der Informationstechnischen Gesellschaft (ITG): Leiter des Fachausschusses 8.1 „Festkörpertechnologie"
- Mitglied der VDE/VDI Gesellschaft für Mikroelektronik, Mikro und Feinwerktechnik (GMM), Leiter des Fachbereichs 1, „Mikro- und Nanoelektronik-Herstellung", Leiter der Fachgruppe 1.2.2 „Ionenimplantation"
- Mitglied des Beirats der Bayerischen Kooperationsinitiative Elektronik / Mikrotechnologie (Bayerisches Staatsministerium für Wirtschaft, Verkehr und Technologie)
- Mitglied der Böhmischen Physikalischen Gesellschaft

Content

Continuation: Participation in Commitees

- Life Fellow of the Institute of Electrical and Electronics Engineers (IEEE)
- Editorial Board of "Radiation Effects and Defects in Solids" Taylor & Francis Ltd., Abingdon, U.K.
- Member of the European SEMI Award Committee
- European Sub-Committee of the International Symposium on VLSI Technology, Systems and Applications (IEEE VLSI-TSA), Taiwan
- Member of the International Advisory Committee of the "International Conference Micro- and Nanoelectronics" (ICMNE)
- Fachkollegiat der DFG im Fachkollegium 408 Elektrotechnik (Stellvertretender Sprecher)

Schellenberger, M.
- Co-Chair der europäischen SEMI PCS-Taskforce
- Mitglied im Programmkomitee und Steeringkomitee der europäischen AEC/APC-Konferenz

Smazinka, T.
- DKE UK 767.3 EMV - Hochfrequente Störgrößen

Conferences, Workshops, Fairs, and Exhibitions

Gemeinsames Kolloquium zur Halbleitertechnologie und Messtechnik von Fraunhofer IISB und Lehrstuhl für Elektronische Bauelemente der Universität Erlangen-Nürnberg (LEB)
IISB, Erlangen, Summer Semester 2011, Winter Semester 2011/2012

Leistungselektronik – Öffentliche Vortragsreihe des Fraunhofer-Innovationsclusters „Elektronik für nachhaltige Energienutzung", Themenschwerpunkt Elektromobilität
IISB, Erlangen, Summer Semester 2011, Winter Semester 2011/2012

QED-Seminar am Clavius-Gymnasium Bamberg
Bamberg, January 15, 2011

Schülerbesuch des Gymnasiums Eckental
IISB, Erlangen, January 27, 2011

DRIVE-E-Akademie 2011
Berlin, February 14 – 18, 2011

Berufsinformationsmesse „realize your visions!" 2011
Nuremberg, February 17, 2011

15. Kooperationsforum des Spitzenclusters „Automation Valley Nordbayern"
Nuremberg, February 18, 2011

Kolloquium am Lehrstuhl für Sensorik der Universität Erlangen-Nürnberg
Erlangen, February 22, 2011

EPCE Workshop on Parasitic effects in power electronics
Berlin, February 23 – 24, 2011

SPIE Advanced Lithography 2011
San José, USA, February 28 – March 4, 2011

14. LEF-Seminar „Laser in der Elektronikproduktion & Feinwerktechnik"
Fürth, March 1, 2011

China Semiconductor Technology International Conference (CSTIC)
Shanghai, China, March 13 - 16, 2011

German Polish Conference on Crystal Growth 2011
Frankfurt / Oder and Slubice, March 14 – 18, 2011

VDE ZVEI Fachgruppentreffen, Applikationsgruppe Automotive
IISB, Erlangen, March 15, 2011

7th International Workshop on Bulk Nitride Semiconductors (ICNS)
Koyasan, Japan, March 15 – 20, 2011

VDMA E-MOTIVE Produktionstechnik Elektromobilität
Frankfurt / Main, March 16, 2011

Treffen der GMM-VDE/VDI-Fachgruppe 1.2.6 „Prozesskontrolle, Inspektion & Analytik"
Regensburg, March 17, 2011

Internationale Fachmesse für Elektromagnetische Verträglichkeit (EMV) 2011
Stuttgart, March 17, 2011

Schülerbesuch des Clavius-Gymnasiums Bamberg
IISB, Erlangen, March 18, 2011

Content

Continuation: Conferences, Workshops, Fairs, and Exhibitions

ECPE Workshop on Power Electronics for Charging Electric Vehicles
Valencia, Spain, March 21 – 22, 2011

Novel High k Applications Workshop
Dresden, March 30, 2011

Hannover Messe
Hannover, April 4 – 8, 2011

Girls' Day – Mädchen-Zukunftstag
IISB, Erlangen, April 14, 2011

Besuch der Deutschen Verkehrswissenschaftlichen Gesellschaft e.V., Bezirksvereinigung Nordbayern
IISB, Erlangen, April 21, 2011

austriamicrosystems Technology Seminar
Unterpremstätten, Austria, April 29, 2011

Festveranstaltung 25 Jahre Solarmobilverein Erlangen
Erlangen, April 30, 2011

Treffen des DGM-AK „Materialien für nichtflüchtige Speicher"
Frankfurt / Oder, May 3, 2011

SEAL General Assembly Meeting
Bergisch Gladbach, May 4, 2011

Märkte der Zukunft – die Automotive-Industrie im Wandel
Passau, May 9, 2011

2011 E-MRS Spring Meeting, Symposium J „Laser materials processing for micro and nano applications"
Strasbourg, France, May 9 – 13, 2011

Fraunhofer-Gutachterausschuss „Interne Programme"
Stuttgart, May 11, 2011

ITG-Fachgruppe 8.1.1 un d GMM-Fachgruppe 1.2.2 – 45. Treffen der Nutzergruppe Ionenimplantation
IISB, Erlangen, May 12, 2011

ITG-Fachgruppe 8.1.2 und der GMM-Fachgruppe 1.2.4 – 29. Treffen der Nutzergruppe Heißprozesse und RTP
IISB, Erlangen, May 12, 2011

Zwischenbegutachtung des Fraunhofer-Innovationsclusters „Elektronik für nachhaltige Energienutzung"
Berlin, May 12 – 13, 2011

Micron Information Seminar
Agrate, Italy, Mai 17, 2011

PCIM 2011
Nuremberg, May 17 – 19, 2011

SPIE Metrology Europe 2011
Munich, May 24, 2011

Kongress Elektromobilität
Berlin, June 1, 2011

IMPROVE WP2/3 meeting
Milano, Italy, June 6, 2011

The 14th International Conference on Total Reflection X-Ray Fluorescence and Related Methods 2011
Dortmund, June 6 – 9, 2011

Besuch einer koreanischen Industriedelegation vermittelt durch das Korea-EU International Cooperation Center (KEUICC)
IISB, Erlangen, June 7, 2011

Workshop "Statistical methods applied in microelectronics"
Milano, Italy, June 13, 2011

112. Jahrestagung der Deutschen Gesellschaft für Angewandte Optik (DGaO)
Ilmenau, June 14 – 18, 2011

CMOS Emerging Technologies Workshop
Whistler, Canada, June 15, 2011

Freiberger Silicon Days 2011
Freiberg, June 15 – 17, 2011

EU-RU.NET Review Meeting
St.Petersburg, Russia, June 24, 2011

Nationale Bildungskonferenz Elektromobilität
Ulm, June 28, 2011

ECPE Workshop on Electronics around the Power Switch: Gate Drivers, Sensors and Control
Munich, June 29 – 30, 2011

ECPE Workshop on Electronics around the power switch: gate drivers, sensors and control
Ismaning, June 29 – 30, 2011

SEAL Review Meeting
Munich, June 30 – July 1, 2011

ENIAC-IMPROVE Joint WP1/WP5 Workshop
Graz, Austria, July 5 – 7, 2011

9th International Conference on Nitride Semiconductors
Glasgow, UK, July 10 – 15, 2011

SEAL project meeting
Landshut, July 11, 2011

Besuch IfKom Ingenieurverband Bezirk Württemberg
IISB, Erlangen, July 11, 2011

BONDING Firmenkontaktmesse
Universität Erlangen-Nürnberg, July 11 – 12, 2011

5. Wissenschaftstag der Metropolregion Nürnberg
Ansbach, July 15, 2011

Abschlussveranstaltung zum Praktikum Mechatronische Systeme im Studiengang Mechatronik der Universität Erlangen-Nürnberg
IISB, Erlangen, July 18, 2011

Schülerbesuch des Melanchthon-Gymnasiums Erlangen
IISB, Erlangen, July 19, 2011

Branchendialog Elektromobilität der Stadt Nürnberg
Nuremberg, July 21, 2011

Schülerbesuch des Emil-von-Behring-Gymnasiums Spardorf
IISB, Erlangen, July 27, 2011

The 18th American Conference on Crystal Growth and Epitaxy (ACCGE)
Monterey, USA, July 31 – August 5, 2011

NAMES AND DATA

Content

Continuation: Conferences, Workshops, Fairs, and Exhibitions

SPIE Optics + Photonics 2011, NanoScience + Engineering, Instrumentation, Metrology, and Standards for Nanomanufacturing, Optics, and Semiconductors V
San Diego, USA, August 21 – 25, 2011

SPIE Optical Design 2011
Marseille, France, September 5 – 7, 2011

8th PAMIR International Conference on Fundamental and Applied MHD
Borgo, France, September 5 – 9, 2011

Praktikum „Mädchen & Technik / Jugend & Technik“
IISB, Erlangen, September 5 – 9, 2011

SISPAD 2011 – International Conference on Simulation of Semiconductor Processes and Devices
Osaka, Japan, September 8 – 10, 2011

International Conference on Silicon Carbide and Related Materials
Cleveland, USA, September 11 – 16, 2011

ESSDERC 2011 – 41st European Solid-State Device Research Conference
Helsinki, Finnland, September 12 – 16, 2011

Chinese-German Young Scientists Forum 2011
Shangai, China, September 14, 2011

9th International Fraunhofer IISB Lithography Simulation Workshop
Hersbruck, September 15 – 17, 2011

Short Course MNE 2011
Berlin, September 19, 2011

GMM-VDE/VDI-Fachgruppe 1.1.3 – 13. Treffen der Nutzergruppe Yield Enhancement
Freiburg, September 19 – 20, 2011

37th International Conference on Micro and Nano Engineering (MNE) 2011
Berlin, September 19 – 23, 2011

SPIE Conference "Photomask Technology"
Monterey, USA, September 20, 2011

14th International Conference on Defects-Recognition, Imaging and Physics in Semiconductors (DRIP-XIV) 2011
Miyazaki, Japan, September 25 – 29, 2011

Herbsttagung Fachgruppe Elektronik und EDV im Bundesverband öffentlich bestellter und vereidigter Sachverständiger e.V. (BVS)
Nuremberg, September 30, 2011

SEAL SP1 Meeting
Leuven, Belgium, October 5, 2011

DGKK-Arbeitskreis „Herstellung und Charakterisierung von massiven Halbleiterkristallen“
IISB, Erlangen, October 5 – 6, 2011

AutoUni Konferenz Hybrid- und Elektrofahrzeuge: Schlüsselfaktoren für die nächste Fahrzeuggeneration
Ingolstadt, October 11, 2011

SEMICON Europa 2011
Dresden, October 11 – 13, 2011

2011 Intel European Research & Innovation Conference (ERIC)
Leixlip, Ireland, October 12 – 14, 2011

SEMICON Europa 2011, 450 mm Conference
Dresden, October 13, 2011

ISMI Manufacturing Week
Austin, TX, USA, October 17 – 20, 2011

eCarTec 2011, 3. Internationale Leitmesse für Elektromobilität
Munich, October 18 – 20, 2011

10th International Conference on Nanoimprint and Nanoprint Technology (NNT) 2011
The Shilla Jeju, Korea, October 19 – 21, 2011

eCarTec 2011, ZVEI Seminar "Experten informieren: Leistungselektronik bewegt die Elektromobilität",
Munich, October 20, 2011

Lange Nacht der Wissenschaften
IISB, Erlangen, October 22, 2011

Verleihung des Innovationspreises Mikroelektronik 2011 des Förderkreises für die Mikroelektronik e.V.
IISB, Erlangen, October 24, 2011

Verleihung des Jugendpreises Mikroelektronik 2011 des Förderkreises für die Mikroelektronik e.V.
IISB, Erlangen, October 24, 2011

General Assembly Meeting EEMI450 Initiative
Leuven, Belgium, October 24, 2011

Urbantec: Smart technologies for better cities
Cologne, October 24 – 26, 2011

Kooperationsforum Bayern-Innovativ mit Fachausstellung Leistungselektronik – Komponenten - Systemintegration - Energieeffizienz
Nuremberg, October 27, 2011

9th Workshop „Beams and More“ 2011
Stuttgart, October 27, 2011

5th International Workshop on Science and Technology of Crystalline Si Solar Cells (CSSC5) 2011
Boston, USA, November 2 – 4, 2011

Erstsemesterexkursion der VDE-Hochschulgruppe ETG Kurzschluss e.V.
IISB, Erlangen, November 9, 2011

ContactING 2011 - 12. Firmenkontaktmesse für Ingenieure und Informatiker
Nuremberg, November 10, 2011

Karlsruhe Institute of Technology (KIT) Seminar
Karlsruhe, November 18, 2011

SEAL General Assembly Meeting
Leuven, Belgium, November 22 – 23, 2011

SEAL Workshop
Leuven, Belgium, November 22 – 23, 2011

ITG-Fachgruppe 8.1.2 und der GMM-Fachgruppe 1.2.4 – 30. Treffen der Nutzergruppe Heißprozesse und RTP
Blaubeuren, November 23, 2011

CONTACT 2011 – 18. Nordbayerische Kontaktmesse für Industrie und Studierende technischer Fachrichtungen
Erlangen, November 23 – 24, 2011

Content

Continuation: Conferences, Workshops, Fairs, and Exhibitions

ITG-Fachgruppe 8.1.1 und GMM-Fachgruppe 1.2.2 – 46. Treffen der Nutzergruppe Ionenimplantation
Blaubeuren, November 24, 2011

Fachtagung Prozessnahe Röntgenanalytik
Berlin, November 24 – 25, 2011

24th Microprocesses and Nanotechnology Conference MNC 2011
Kyoto, Japan, November 24 – 27, 2011

Zeiss-SMT Fachseminar
Oberkochen, November 25, 2011

GMM-VDE/VDI-Fachgruppe 1.2.3 – Treffen der Nutzergruppe Abscheide- und Ätzverfahren „PVD & PECVD und Ätzen"
IISB, Erlangen, December 6, 2011

GMM-VDE/VDI-Fachgruppe 1.2.3 – Workshop der Nutzergruppe Abscheide- und Ätzverfahren „New developments and process optimization in deposition and etching"
IISB, Erlangen, December 7, 2011

13th Fraunhofer IISB Annual Conference – Technology Simulation
IISB, Erlangen, December 9, 2011

Winter Simulation Conference (WSC) 2011
Phoenix, USA, December 11 – 14, 2011

2011 ITRS Winter Public Conference
Incheon, Korea, December 14, 2011

10th Indo-German Winter Academy
Surajkund, India, December 15, 2011

Verleihung der IISB-Forschungs und Entwicklungspreise 2011
IISB, Erlangen, December 20, 2011

Publications

Agudelo, V., Evanschitzky, P., Erdmann, A., Führer, T., Shao, F., Limmer, S., Fey,D.:
Accuracy and performance of 3D mask models in optical projection lithography
Proceedings, SPIE Advanced Lithography 2011, 7973, 797300, 2011

Azizi, M., Meissner, E., Friedrich, J., Müller, G.:
Liquid phase epitaxy (LPE) of GaN on c-and r-faces of AlN substrates
Journal of Crystal Growth 322, 1, 74, 2011
DOI: 10.1016/j.jcrysgro.2011.03.014

Bakowskie, R., Petter, K., Eiternick, S., Lausch, D., Müller, G.:
Efficient methods for detection of SiC and Si3N4 precipitates and filaments in multi-crystalline silicon wafers and solar cells
Phys. Status Solidi C 8, 4, 1380, 2011

Bramati, A., Vogler, U., Meliorisz, B., Motzek, K., Hornung, M., Voelkel, R.:
Simulation tools for advanced mask aligner lithography
Proceedings, SPIE Optical System Design 2011, 8167, 81670U
DOI: 10.1117/12.897572

Cao, Y., Wang, X., Erdmann, A., Bu, P., Bu, Y.:
Analytical model for EUV mask diffraction field calculation
Proceedings, SPIE Optical Design 2011, 8171, 81710N, 2011
DOI: 10.1117/12.896579

Codegoni, D., Polignano, M. L., Castellano, L., Borionetti, G., Bonoli, F., Nutsch, A., Leibold, A., Otto, M.:
The impact of organic contamination on the oxide-silicon interface
Proceedings, American Institute of Physics (AIP), 1395, 217, 2011
DOI: http://link.aip.org/link/doi/10.1063/1.3657894?ver=pdfcov

Dadzis, K., Ehrig, J., Niemietz, K., Pätzold, O., Wunderwald, U., Friedrich, J.:
Model experiments and numerical simulations for directional solidification of multicrystalline silicon in a traveling magnetic field
Journal of Crystal Growth 333, 1, 7, 2011
DOI: 10.1016/j.jcrysgro.2011.08.009

SCIENTIFIC PUBLICATIONS

Content

Continuation: Publications

Dadzis, K., Zschorsch, M., Wunderwald, U., Jung, T., Friedrich, J.:
Three-dimensional modeling of melt flow in directional solidification of large multi-crystalline silicon ingots with a travelling magnetic field
Journal of Crystal Growth 333, 7–15, 2011

Daves, W., Krauss, A., Behnel, N., Häublein, V., Bauer, A., Frey, L.:
Amorphous silicon carbide thin films (a-SiC:H) deposited by plasma-enhanced chemical vapor deposition as protective coatings for harsh environment applications
Thin solid films 519 (2011), 18, 5892, 2011
DOI: 10.1016/j.tsf.2011.02.089

Daves, W., Krauss, A., Le-Huu, M., Kronmüller, S., Häublein, V., Bauer, A.J., Frey, L.:
Comparative study on metallization and passivation materials for high temperature sensor applications
Selected, peer reviewed papers from the 8th European Conference on Silicon Carbide and Related Materials (ECSCRM) 2010, Trans Tech Publications, 2011, 449, 2011
and
Materials Science Forum 679/680, 2011
DOI: 10.4028/www.scientific.net/MSF.679-680.449

Daves, W., Krauss, A., Häublein, V., Bauer, A. J., Frey, L.:
Enhancement of the stability of Ti and Ni ohmic contacts to 4H-SiC with a stable protective coating for harsh environment applications
Journal of Electronic Materials 40, 9, 1990, 2011
DOI: 10.1007/s11664-011-1681-2

Dorp, J. vom, Erlbacher, T., Bauer, A. J., Ryssel, H., Frey, L.:
Dielectric layers suitable for high voltage integrated trench capacitors
Journal of vacuum science and technology B. Microelectronics and nanometer structures, 29, 1, 01AB04, 2011
DOI: 10.1116/1.3525283

Dorp, J. vom, Berberich, S., Erlbacher, T., Bauer, A. J., Ryssel, H., Frey, L.:
Monolithic RC-snubber for power electronic applications
Proceedings, IEEE 9th International Conference on Power Electronics and Drive Systems (PEDS) 2011, 11, 2011
DOI: 10.1109/PEDS.2011.6147217

Erdmann, A., Shao, F., Agudelo, V., Fühner, T., Evanschitzky, P.:
Modeling of mask diffraction and projection imaging for advanced optical and EUV lithography
Journal of modern optics, 58, No.5&6, 480, 2011
DOI: 10.1080/09500340.2010.515752

Erdmann, A., Evanschitzky, P., Shao, F., Fühner, T., Lorusso, G., Hendrickx, E., Goethals, A. M., Jonckheere, R., Bret, T., Hofmann, T.:
Predictive modeling of EUV-lithography: The role of mask, optics, and photoresist effects
Proceedings, SPIE Optical Design 2011, 8171, 81710M, 2011
DOI: 10.1117/12.896813

Erlbacher, T., Yanev, V., Rommel, M., Bauer, A.J., Frey, L.:
Gate oxide reliability at the nano-scale evaluated by combining cAFM and CVS
Journal of vacuum science and technology B. Microelectronics and nanometer structures, 29, 1, 01AB08, 2011
DOI: 10.1116/1.3532820

Evanschitzky, P., Shao, F., Fühner, T., Erdmann, A.:
Compensation of mask induced aberrations by projector wavefront control
Proceedings, SPIE Advanced Lithography 2011, 7973, 797329, 2011

Evanschitzky, P., Fühner, T., Erdmann, A.:
Image simulation of projection systems in photolithography
Proceedings, SPIE 2011, Modeling aspects in optical metrology III, Optical Metrology Symposium, 8083, 80830E, 2011
DOI: 10.1117/12.895029

Fet, A., Häublein, V., Bauer, A. J., Ryssel, H., Frey, L.:
Fluorine implantation for effective work function control in p-type metal-oxide-semiconductor high-k metal gate stacks
Journal of vacuum science and technology B, Microelectronics and nanometer structures 29, 1, 01A905, 2011
DOI: 10.1116/1.3521471

Content

Continuation: Publications

Fried, M., Juhasz, G., Major, C., Petrik, P., Polgar, O., Horvath, Z., Nutsch, A.:
Expanded beam (macro-imaging) ellipsometry
Proceedings, 5th International Conference on Spectroscopic Ellipsometry (ICSE) 2011, 2730, 2011
and
Thin solid films 519, 9, 2011
DOI: 10.1016/j.tsf.2010.12.067

Friedrich, J., Müller, G.:
Kristalle - Wunderwerkstoffe für die Industrie
Technologisch! Technologien erfolgreich in den Markt bringen, Editor: Bullinger, Hans-Jörg, 105 – 118, 2011

Hourdakis, E., Nassiopoulou, A. G., Parisini, A., Reading, M. A., van den Berg, J.A., Sygellou, L., Ladas, S., Petrik, P., Nutsch, A., Wolf, M., Roeder, G.:
Electrical and structural properties of ultrathin SiON films on Si prepared by plasma nitridation
Journal of Vacuum Science & Technology B, 29, 022201, 2011
DOI: 10.1116/1.3556938

Jambreck, J. D., Yanev, V., Schmitt, H., Rommel, M., Bauer, A.J., Frey, L.:
Manufacturing, characterization, and application of nanoimprinted metallic probe demonstrators for electrical scanning probe microscopy
Journal of Microelectronic Engineering, 88, 2584, 2011
DOI: 10.1016/j.mee.2010.12.022

Jambreck, J. D., Böhmler, M., Rommel, M., Hartschuh, A., Bauer, A. J., Frey, L.:
Light confinement by structured metal tips for antenna-based scanning near-field optical microscopy
Proceedings, SPIE Conference "Instrumentation, Metrology, and Standards for Nanomanufacturing, Optics, and Semiconductors V", 8105, 81050G, 2011
DOI: 10.1117/12.893306

Kaiser, R. J., Koffel, S., Pichler, P., Bauer, A. J., Amon, B., Frey, L., Ryssel, H.:
Germanium substrate loss during thermal processing
Microelectronic Engineering 88, 499-502, 2011

Kalai Selvi, K., Sreenidhi, T., Dasgupta, N., Ryssel, H., Bauer, A.:
High pressure oxidation of 4H-SiC in nitric acid vapor
Japanese journal of applied physics, 2, 50, 10, 2011
DOI: 10.1143/JJAP.50.10PG07

Kallinger, B., Thomas, B., Berwian, P., Friedrich, J., Trachta, G., Weber, A.-D.:
4H-SiC homoepitaxial growth on substrates with different off-cut directions
Selected, peer reviewed papers from the 8th European Conference on Silicon Carbide and Related Materials (ECSCRM) 2010, Trans Tech Publications, 2011, 55, 2011
and
Materials Science Forum 679/680, 55, 2011
DOI: http://dx.doi.org/10.4028/www.scientific.net/MSF.679-680.55

Kallinger, B., Polster, S., Berwian, P., Friedrich, J., Müller, G., Danilewsky, A. N., Wehrhahn, A., Weber, A.-D.:
Threading dislocations in n- and p-type 4H-SiC material analyzed by etching and synchrotron x-ray topography
Journal of Crystal Growth, 314, 1, 21, 2011
DOI: 10.1016/j.jcrysgro.2010.10.145

Kallinger, B., Polster, S., Berwian, P., Friedrich, J., Müller, G., Danilewsky, A., Wehrhahn, A., Weber, A.-D.:
Dislocation Types and Densities of 4H-SiC Substrates and Homoepitaxial Layers Analyzed by Etching and Synchrotron X-Ray Topography
Journal of Crystal Growth, 314, 21, 2011

Kampen, C., Burenkov, A., Pichler, P., Lorenz, J.:
On the influence of RTA and MSA peak temperature variations on Schottky contact resistances of 6-TSRAM cells
Solid-State Electronics, 65-66, 114, 2011
DOI: http://dx.doi.org/10.1016/j.sse.2011.06.005

Content

Continuation: Publications

Kampen, C., Burenkov, A., Lorenz, J.:
Challenges in TCAD simulations of tunneling field effect transistors
Proceedings, 41st European Solid-State Device Research Conference (ESSDERC) 2011, 139, 2011
DOI: 10.1109/ESSDERC.2011.6044215

Knoerr, M., Schletz, A.:
Power semiconductor joining through sintering of silver nanoparticles: Evaluation of influence of parameters time, temperature and pressure on density, strength and reliability
Proceedings, 6th International Conference on Integrated Power Electronics Systems (CIPS) 2010, 5730660, 2011

Koffel, S., Kaiser, R.J., Bauer, A. J., Amon, B., Pichler, P., Lorenz, J., Frey, L., Scheiblin, P., Mazzocchi, V., Barnes, J.-P., Claverie, A.:
Experiments and simulation of the diffusion and activation of the n-Type dopants P, As, and Sb implanted into germanium
Microelectronic Engineering 88, 458, 2011
DOI: http://dx.doi.org/10.1016/j.mee.2010.09.023

Körmer, R., Otto, M., Wu, J., Jank, M. P. M., Frey, L., Peukert, W.:
EPR investigations of non-oxidized silicon nanoparticles from thermal pyrolysis of silane
Physica status solidi, Rapid research letters 5, 7, 244, 2011
DOI: 10.1002/pssr.201105208

Koitzsch, M., Schellenberger, M.:
Thermal Laser Separation (TLS) for Separating Multi-Crystalline Silicon Wafers: a Comparison with State-of-the-Art Methods
26th European Photovoltaic Solar Energy Conference and Exhibition, 2011

Koitzsch, M., Honold, A.:
Evaluation of Economic Effects as the Basis for Assessing Virtual Metrology Investment
Future Fab International, 37, May 2011

Koitzsch, M., Merhof, J., Michl, M., Noll, M., Nemecek, A., Honold, A., Kleineidam, G., Lebrecht, H.:
Implementing Virtual Metrology into Semiconductor Production Processes - An Investment Assessment
Proceedings, the 2011 Winter Simulation Conference, Phoenix, USA, 2011
DOI: 10.1109/WSC.2011.6147915

Kozawa, T., Erdmann, A.:
Feasibility study of chemically amplified resists for short wavelength extreme ultraviolet lithography
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